Kneron KL720 series AI SoC

Data Sheet

2021 May.

Version 1.0

Revision History:

version	Description	date
0.1	Initial version	2020/01/05
0.2	Package data	2020/05/31
0.3	Power list	2020/09/28
0.4	Power supply pin VCC18A_TDC0 of 9x9	2020'10/12
0.5	Always-on Power list	2020/11/06
0.6	X_PSW_BAS – Power up Sequence	2020/11/13
0.7	Chap 5. Electrical Characteristic Add 6. Thermal information Add 9.1 Reflow information	2020/11/30
0.8	Table 10, correct VCCK_NPU naming	2020/12/23
1.0	(1) Table 6, modify description of VCC12A_MPRX0 & VCC12A_MPRX1 & VDD1_KGD18A (2) Table 27, update the description (3) update section 1.1and 1.2 (4) Add section 2.16 (5) add section 7.1 (6) Update section 8	2021/5/26

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1. Overview

1.1 General description

Kneron KL720 series is an AI SoC targeting smart-home and IoT segment with Kneron NPU core inside to accelerate neural network processing and enabling devices with edge AI ability to achieve Kneron's AI everywhere vision.

The NPU core is designed to accelerate major computing layers inside the convolutional neural network (CNN) and recurrent neural network (RNN), to off-load the heavy computing from traditional CPU or GPU structure. So, our AI SoC can achieve edge side AI computing with only entry level MCU accompanied with Kneron NPU core in order to save development cost. Kneron KL720 series AI SoC is suitable for access control, smart retail, surveillance AI camera, home appliance.

1.2 Key specification

NPU

- Maximum Frequency @ 696 MHz
- Peak Throughput of 8-bit mode: 1425 GOPS, 1024MAC/cycle

CPU

- ARM Cortex-M4@400MHz for system control

DSP

- Tensilica DSP @ 500Mhz for AI assistance

SDRAM

- SIP, 128MB, 32-bit LPDDR3-2133

External flash

- Up to 128 MB SPI NOR or NAND flash

Supporting OS

- CMSIS RTX

Power

- Average power consumption: 1.725W@Yolov3_608
  - Activity condition: NPU, DSP, LPDDR3, USB3 device
  - 0.9V core voltage and 1.8V/3.3V I/O voltage (grouped by IO banks)

Video in interface

- 2-lane MIPI-CSI-2 RX
- DVP

Video out interface

- DVP
- LCM
- SPI

Audio Interface

- I2S

Peripheral Interface

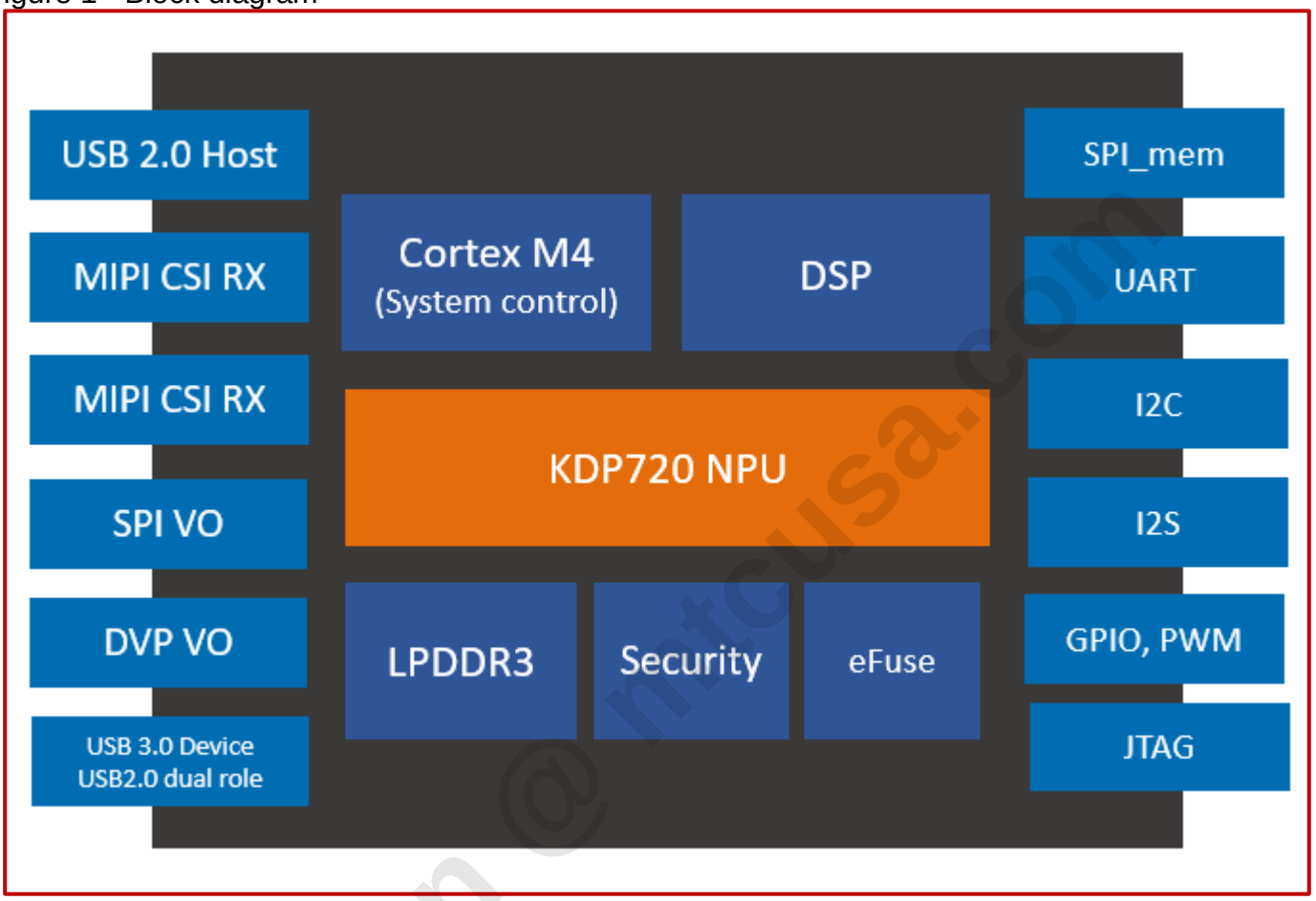
- I2C

- SPI
- UART
- USB 3.0 device interface
- USB 2.0 host interface
- PWM
- GPIO
- SDIO
- SDCARD
- Dual JTAG interface

1.3 Block diagram

Here is the KL720 system block diagram. Which descripted the dedicated component for AI SoC indicator.

Figure 1 - Block diagram



2. Functional Description

2.1 CPU

In order to get the optimized performance and efficiency, there is one Cortex-M4 embedded in KL720-series. System CPU is designed for the chip operation which is equipped with i-mem of 128KB and d-mem of 128KB. Major work items are serviced RTOS, IO driver, video input and output, 3rd party application.

2.2 NPU

Kneron's self-developed 2nd generation NPU is embedded in KL720-series. Its lego-like architecture services popular CNN models such as Yolo, Resnet, Mobilenet and Mobilenet-SSD. It supports reconfigurable mechanism by INT8 or INT16 hybrid precisions. The inference AI model can be updated by OTA.

2.3 DSP

AI computing DSP is used to execute computer vision pre-processing and post-processing functions, while NPU handles AI computations. The Licensed toolchain from Cadence is used to build DSP code like a general-purpose DSP.

2.4 DRAM

LPDDR3 is embedded in KL720-series to reduce the power consumption. There is single option to use 128MB.

2.5 MIPI CSI RX

KL720-series provides a high-resolution, high-speed and flexible interconnect of the MIPI CSI receiver. It is compliant with the Camera Serial Interface 2 (CSI-2) and supports the MIPI Alliance specifications. The supported data rate is up to 1.2 Gbps per data lane and it is scalable from one to two data lanes

2.6 DVP video interface

To link with the general parallel video interfaces in the market, KL720-series provides parallel input / output interface by RGB format (RGB-888 / RGB-565) and YUV format (YUV422).

2.7 I2C

I2C in KL720-series is configurable to be able to serve as a master or slave residing on the I2C bus. The master is a device that initiates the data transfers on the bus and generates the clock signals to permit the transfers. During these transfers, any addressed device is considered a slave. Data are transmitted and received from the I2C bus through a buffered interface. Two wires, the serial data (SDA) and serial clock (SCL), carry information between devices connected to the bus.

2.8 I2S

Since I2S is a populate audio format provided by many audio devices, KL720-series provides this interface to transfer digital audio data.

2.9 UART

UART in KL720-series implements the most common communications protocols. In UART mode of operation it is backward compatible to the 16550 to support existing communication software.

2.10 USB

There are 2 USB ports. One USB 3.0 in KL720-series can be configured as device only. One USB 2.0 in KL720-series can be configured as host only.

USB controller features:

- Compliance with USB-IF
- Support control, bulk and interrupt transfer
- Support UVC in limited function
- Internal DMA mode for efficient data transfer

2.11 SPI

There are 3 kinds of SPI in KL720-series. It contains SPI interface controller to execute the SPI Flash command as ROM and link with other devices. The other SPI interface supports the display or video output. The last one is general SPI for BT or wireless device.

2.12 GPIO

KL720-series provides a flexible, configurable and programmable general-purpose I/O. The options to remove or add the interrupt sense, bouncing clock, and pull high/low circuits are programable. The attributes of each GPIO pin, such as input/output, bypass, interrupt sense, clock source, and pull type can be programmed to fit the user specification. GPIO also provides a bouncing clock to be used for the de-bounce input.

2.13 SDIO

KL720-series has a host controller of the SD (Secure Digital) interface which is compliant with the SD physical layer specification, version 2.0.

2.14 Security Engine

Support security boot and normal boot.
eFuse major

- Support hash algorithm for Public key
- Code encryption key
- Firmware version counter
- Bit map: 512b, 128b

Public Key recommends

- security boot: 128 bits

Code encryption key

- AES: 128 bits

Firmware image rollback counter

- At least 32 bits

Block Cipher Algorithms

- AES: ECB, CBC, CTR, OFB
- DES: ECB, CBC ECB, CBC

Digest Algorithms

- HASH: MD5
- AES: XCBC

Authenticated Encryption Algorithms

Authenc (XCBC, CBC)

Figure 2 - Security boot flow-I

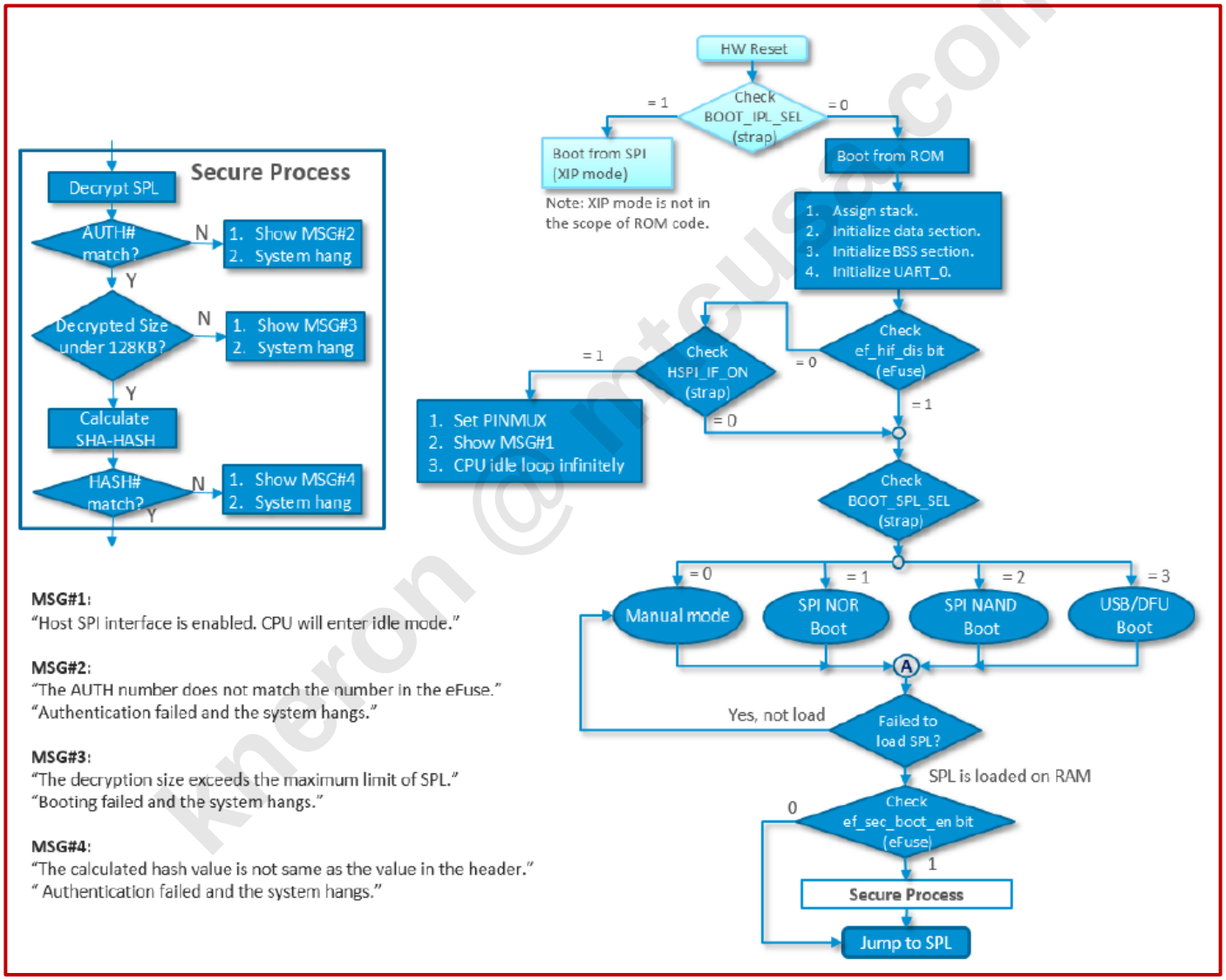
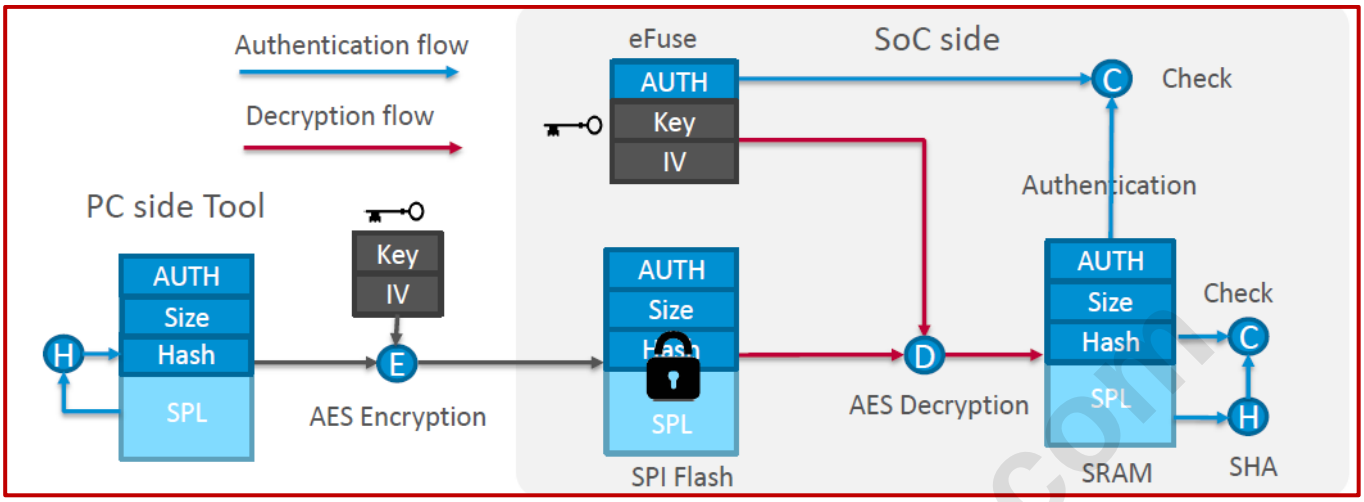


Figure 3 - security boot flow-II



2.15 PWM

KL720-series's internal timer supports the PWM (Pulse Width Modulation) function to generate the PWM signals for the motor control or power level control.

2.16 Package

KL720-series support 2 kinds of package – 9x9 and 11x11. There are several different points between 9x9 and 11x11 as below.

- Package size
- IO pin assignment. The sensors interface (MIPI and DVP) only be enabled on 11x11. The numbers of GPIO pin in the package 11x11 also bigger than 9x9.

Please refer the section3.1 for detail description.

3. Pin Descriptions

3.1 IO list

Table 1 - IO list

Feature	9x9 Package	11x11 Package
SPI-Flash	1	1
I2C	2	3
SPI(SSP1)	0	1
I2S(SSP0)	1	1
SD-CARD	1	1
SD_IO	1	1
DPI In	0	1
DPI Out	1	1
UART	2	2
JTAG	1	1
PWM	2	2
DSP JTAG	0	1
GPIO (shared)	21	32
MIPI-RX1 (2 lanes)	0	1
MIPI-RX1 (2 lanes)	0	1
USB2 Host	1	1
USB3 Device	1	1
Embedded DDR	1	1
RTC	1	1

3.2 Pin mux table

Table 2 - Pin mux table 1/2

IO Port Name	PKG 9x9	PKG 11x11	IO Bank	Mode0	DIR	Mode1	DIR	Mode2	DIR	Mode3	DIR
X_DPI_PCLKI		V	Bank0 by ExtReg	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I
X_DPI_VSI		V		DPI_VSI	I	DPI_VSI	I	DPI_VSI	I	DPI_VSI	I
X_DPI_HSI		V		DPI_HSI	I	DPI_HSI	I	DPI_HSI	I	DPI_HSI	I
X_DPI_DEI		V		DPI_DEI	I	DPI_DEI	I	DPI_DEI	I	DPI_DEI	I
X_DPI_DATAI[0]		V		DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I
X_DPI_DATAI[1]		V		DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I
X_DPI_DATAI[2]		V		DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I
X_DPI_DATAI[3]		V		DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I
X_DPI_DATAI[4]		V		DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I
X_DPI_DATAI[5]		V		DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I
X_DPI_DATAI[6]		V		DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I
X_DPI_DATAI[7]		V		DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I
X_DPI_DATAI[8]		V		DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I
X_DPI_DATAI[9]		V		DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I
X_DPI_DATAI[10]		V		DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I
X_DPI_DATAI[11]		V		DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I
X_DPI_DATAI[12]		V		DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I
X_DPI_DATAI[13]		V		DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I
X_DPI_DATAI[14]		V		DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I
X_DPI_DATAI[15]		V		DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I
X_SPI_CS_N	V	V	Bank1 by IO	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O
X_SPI_CLK	V	V		SPI_CLK	O	SPI_CLK	O	SPI_CLK	O	SPI_CLK	O
X_SPI_DO	V	V		SPI_DO	O	SPI_DO	O	SPI_DO	O	SPI_DO	O
X_SPI_DI	V	V		SPI_DI	I	SPI_DI	I	SPI_DI	I	SPI_DI	I
X_SPI_WP_N	V	V		SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O
X_SPI_HOLD_N	V	V		SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O
X_I2C0_CLK	V	V		I2C0_CLK	I/O	I2C0_CLK	I/O	I2C0_CLK	I/O	1'b0	I
X_I2C0_DATA	V	V		I2C0_DATA	I/O	I2C0_DATA	I/O	I2C0_DATA	I/O	1'b0	I
X_MCLK	V	V		MCLK	O	MCLK	O	MCLK	O	MCLK	O
X_SSP0_CLK	V	V		SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O
X_SSP0_CS0	V	V		SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O
X_SSP0_CS1		V		SSP0_CS1	I/O	SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I
X_SSP0_DI	V	V		SSP0_DI	I	SSP0_DI	I	SSP0_DI	I	SSP0_DI	I
X_SSP0_DO	V	V		SSP0_DO	O	SSP0_DO	O	SSP0_DO	O	SSP0_DO	O
X_UART0_TX	V	V		UART0_TX	O	UART1_TX	O	UART1_TX	O	UART1_TX	O
X_UART0_RX	V	V		UART0_RX	I	UART1_RX	I	UART1_RX	I	1'b0	I
X_TRACE_CLK		V		Reserve	O	UART1_DCD	I	UART1_DCD	I	1'b0	I
X_TRACE_DATA[0]		V		Reserve	O	UART1_DTR	O	UART1_DTR	O	1'b0	I
X_TRACE_DATA[1]		V		Reserve	O	UART1_DSR	I	UART1_DSR	I	1'b0	I
X_TRACE_DATA[2]		V		Reserve	O	UART1_RTS	O	UART1_RTS	O	1'b0	I
X_TRACE_DATA[3]		V		Reserve	O	UART1_CTS	I	UART1_CTS	I	UART1_CTS	I
X_UART1_RI		V		UART1_RI	I	UART1_RI	I	UART1_RI	I	UART1_RI	I
X_I2C1_CLK	V	V	Bank3 by ExtReg	I2C1_CLK	I/O	I2C1_CLK	I/O	I2C1_CLK	I/O	1'b0	I
X_I2C1_DATA	V	V		I2C1_DATA	I/O	I2C1_DATA	I/O	I2C1_DATA	I/O	1'b0	I
X_SSP1_CLK	V	V		SSP1_CLK	I/O	DPI_DATAO[13]	O	SSP1_CLK	I/O	SSP1_CLK	I/O

IO Port Name	PKG 9x9	PKG 11x11	IO Bank	Mode0	DIR	Mode1	DIR	Mode2	DIR	Mode3	DIR
X_SSP1_CS	V	V		SSP1_CS	I/O	DPI_DATAO[14]	O	SSP1_CS	I/O	SSP1_CS	I/O
X_SSP1_DI	V	V		SSP1_DI	I	DPI_DATAO[15]	O	SSP1_DI	I	SSP1_DI	I
X_SSP1_DO	V	V		SSP1_DO	O	DPI_DATAO[16]	O	SSP1_DO	O	SSP1_DO	O
X_SSP1_DCX	V	V		SSP1_DCX	O	DPI_DATAO[17]	O	SSP1_DCX	O	SSP1_DCX	O
X_PWM1	V	V		PWM1	O	PWM1	O	DSP_JTAG_TDO	O	DPI_DATAO[12]	I
X_DPI_PCLKO	V	V		DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O
X_DPI_VSO	V	V		DPI_VSO	O	DPI_VSO	O	DPI_VSO	O	DPI_VSO	O
X_DPI_HSO	V	V		DPI_HSO	O	DPI_HSO	O	DPI_HSO	O	DPI_HSO	O
X_DPI_DEO	V	V		DPI_DEO	O	DPI_DEO	O	DPI_DEO	O	DPI_DEO	O
X_DPI_DATAO[0]	V	V		DPI_DATAO[0]	O	DSP_JTAG_TRST_N	I	DPI_DATAO[0]	O	DPI_DATAO[0]	O
X_DPI_DATAO[1]	V	V		DPI_DATAO[1]	O	DSP_JTAG_TDI	I	DPI_DATAO[1]	O	DPI_DATAO[1]	O
X_DPI_DATAO[2]	V	V		DPI_DATAO[2]	O	DSP_JTAG_TMS	I	DPI_DATAO[2]	O	DPI_DATAO[2]	O
X_DPI_DATAO[3]	V	V		DPI_DATAO[3]	O	DSP_JTAG_TCK	I	DPI_DATAO[3]	O	DPI_DATAO[3]	O
X_DPI_DATAO[4]	V	V		DPI_DATAO[4]	O	UART1_TX	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O
X_DPI_DATAO[5]	V	V		DPI_DATAO[5]	O	UART1_RX	I	DPI_DATAO[5]	O	DPI_DATAO[5]	O
X_DPI_DATAO[6]	V	V		DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O
X_DPI_DATAO[7]	V	V		DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O
X_DPI_DATAO[8]	V	V		DPI_DATAO[8]	O	DPI_DATAO[8]	O	DPI_DATAO[8]	O	DPI_DATAO[8]	O
X_DPI_DATAO[9]	V	V		DPI_DATAO[9]	O	DPI_DATAO[9]	O	DPI_DATAO[9]	O	DPI_DATAO[9]	O
X_DPI_DATAO[10]	V	V		DPI_DATAO[10]	O	DPI_DATAO[10]	O	DPI_DATAO[10]	O	DPI_DATAO[10]	O
X_DPI_DATAO[11]	V	V		DPI_DATAO[11]	O	DPI_DATAO[11]	O	DPI_DATAO[11]	O	DPI_DATAO[11]	O
X_I2C2_CLK		V	Bank2 by IO	I2C2_CLK	I/O	I2C2_CLK	I/O	I2C2_CLK	I/O	1'b0	I
X_I2C2_DATA		V		I2C2_DATA	I/O	I2C2_DATA	I/O	I2C2_DATA	I/O	1'b0	I
X_DSP_TRSTN	V	V		DSP_JTAG_TRST_N	I	UART0_TX	O	UART0_TX	O	1'b0	I
X_DSP_TDI	V	V		DSP_JTAG_TDI	I	UART0_RX	I	UART0_RX	I	1'b0	I
X_DSP_TDO		V		DSP_JTAG_TDO	O	UART0_IRDA_RX_H	I	UART0_IRDA_RX_H	I	1'b0	I
X_DSP_TMS		V		DSP_JTAG_TMS	I	UART0_IRDA_RX_L	I	UART0_IRDA_RX_L	I	1'b0	I
X_DSP_TCK		V		DSP_JTAG_TCK	I	UART0_IRDA_TX	O	UART0_IRDA_TX	O	MCU_JTAG_TDO	O
X_PWM0	V	V		PWM0	O	PWM0	O	PWM0	O	1'b0	I
X_JTAG_TRSTN	V	V	Bank4 (3.3V)	MCU_JTAG_TRST_N	I	HSPI_CLK	I	HSPI_CLK	I	1'b0	I
X_JTAG_TDI	V	V		MCU_JTAG_TDI	I	HSPI_CS	I	HSPI_CS	I	1'b0	I
X_JTAG_TMS	V	V		MCU_JTAG_TMS	I	HSPI_DI	I	HSPI_DI	I	1'b0	I
X_JTAG_TCK	V	V		MCU_JTAG_TCK	I	HSPI_DO	O	HSPI_DO	O	1'b0	I
X_SD1_D3	V	V		SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O
X_SD1_D2	V	V		SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O
X_SD1_D1	V	V		SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O
X_SD1_D0	V	V		SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O
X_SD1_CMD	V	V		SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O
X_SD1_CLK	V	V		SD1_CLK	O	SD1_CLK	O	SD1_CLK	O	SD1_CLK	O
X_SD0_D3	V	V		SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O
X_SD0_D2	V	V		SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O
X_SD0_D1	V	V		SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O
X_SD0_D0	V	V		SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O
X_SD0_CMD	V	V		SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O
X_SD0_CLK	V	V		SD0_CLK	O	SD0_CLK	O	SD0_CLK	O	SD0_CLK	O
X_SD0_CARD_PWN	V	V		SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	SD0_CARD_PWREN	O
X_SD0_CARD_DET	V	V		SD0_CARD_DET	I	SD0_CARD_DET	I	SD0_CARD_DET	I	SD0_CARD_DET	I
X_JTAG_TDO	V	V		MCU_JTAG_TDO	O	SD0_W_PORT	I	SD0_W_PORT	I	SD0_W_PORT	I

Table 3 - Pin mux table 1/2

IO Port Name	PKG 9x9	PKG 11x11	IO Bank	Mode4	DIR	Mode5	DIR	Mode6	DIR	Mode7	DIR
X_DPI_PCLKI		V	Bank0 by ExtReg	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I	DPI_PCLKI	I
X_DPI_VSI		V		DPI_VSI	I	DPI_VSI	I	DPI_VSI	I	DPI_VSI	I
X_DPI_HSI		V		DPI_HSI	I	DPI_HSI	I	DPI_HSI	I	DPI_HSI	I
X_DPI_DEI		V		DPI_DEI	I	DPI_DEI	I	DPI_DEI	I	DPI_DEI	I
X_DPI_DATAI[0]		V		DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I	DPI_DATAI[0]	I
X_DPI_DATAI[1]		V		DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I	DPI_DATAI[1]	I
X_DPI_DATAI[2]		V		DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I	DPI_DATAI[2]	I
X_DPI_DATAI[3]		V		DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I	DPI_DATAI[3]	I
X_DPI_DATAI[4]		V		DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I	DPI_DATAI[4]	I
X_DPI_DATAI[5]		V		DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I	DPI_DATAI[5]	I
X_DPI_DATAI[6]		V		DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I	DPI_DATAI[6]	I
X_DPI_DATAI[7]		V		DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I	DPI_DATAI[7]	I
X_DPI_DATAI[8]		V		DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I	DPI_DATAI[8]	I
X_DPI_DATAI[9]		V		DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I	DPI_DATAI[9]	I
X_DPI_DATAI[10]		V		DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I	DPI_DATAI[10]	I
X_DPI_DATAI[11]		V		DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I	DPI_DATAI[11]	I
X_DPI_DATAI[12]		V		DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I	DPI_DATAI[12]	I
X_DPI_DATAI[13]		V		DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I	DPI_DATAI[13]	I
X_DPI_DATAI[14]		V		DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I	DPI_DATAI[14]	I
X_DPI_DATAI[15]		V		DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I	DPI_DATAI[15]	I
X_SPI_CS_N	V	V	Bank1 by IO	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O	SPI_CS_N	O
X_SPI_CLK	V	V		SPI_CLK	O	SPI_CLK	O	SPI_CLK	O	SPI_CLK	O
X_SPI_DO	V	V		SPI_DO	O	SPI_DO	O	SPI_DO	O	SPI_DO	O
X_SPI_DI	V	V		SPI_DI	I	SPI_DI	I	SPI_DI	I	SPI_DI	I
X_SPI_WP_N	V	V		SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O	SPI_WP_N	O
X_SPI_HOLD_N	V	V		SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O	SPI_HOLD_N	O
X_I2C0_CLK	V	V		PWM0	O	I2C0_CLK	I/O	CORE_DBG_0	O	GPIO_0	I/O
X_I2C0_DATA	V	V		PWM1	O	I2C0_DATA	I/O	CORE_DBG_1	O	GPIO_1	I/O
X_MCLK	V	V		MCLK	O	MCLK	O	MCLK	O	MCLK	O
X_SSP0_CLK	V	V		SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O	SSP0_CLK	I/O
X_SSP0_CS0	V	V		SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O	SSP0_CS0	I/O
X_SSP0_CS1		V		SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I	SSP0_CS1	I/O
X_SSP0_DI	V	V		SSP0_DI	I	SSP0_DI	I	SSP0_DI	I	SSP0_DI	I
X_SSP0_DO	V	V		SSP0_DO	O	SSP0_DO	O	SSP0_DO	O	SSP0_DO	O
X_UART0_TX	V	V		UART1_TX	O	UART1_TX	O	CORE_DBG_15	O	GPIO_15	I/O
X_UART0_RX	V	V		UART1_RX	I	UART1_RX	I	CORE_DBG_16	O	GPIO_16	I/O
X_TRACE_CLK		V		UART1_DCD	I	UART1_DCD	I	CORE_DBG_17	O	GPIO_17	I/O
X_TRACE_DATA[0]		V		UART1_DTR	O	UART1_DTR	O	CORE_DBG_18	O	GPIO_18	I/O
X_TRACE_DATA[1]		V		UART1_DSR	I	UART1_DSR	I	CORE_DBG_19	O	GPIO_19	I/O
X_TRACE_DATA[2]		V		UART1_RTS	O	UART1_RTS	O	CORE_DBG_20	O	GPIO_20	I/O
X_TRACE_DATA[3]		V		UART1_CTS	I	UART1_CTS	I	CORE_DBG_21	O	GPIO_21	I/O
X_UART1_RI		V		UART1_RI	I	UART1_RI	I	CORE_DBG_22	O	GPIO_22	I/O
X_I2C1_CLK	V	V	Bank3 by ExtReg	UART0_TX	O	MCU_JTAG_TRST_N	I	CORE_DBG_2	O	GPIO_2	I/O
X_I2C1_DATA	V	V		UART0_RX	I	MCU_JTAG_TDI	I	CORE_DBG_3	O	GPIO_3	I/O
X_SSP1_CLK	V	V		SSP1_CLK	I/O	SSP1_CLK	O	SSP1_CLK	I/O	SSP1_CLK	I/O
X_SSP1_CS	V	V		SSP1_CS	I/O	SSP1_CS	O	SSP1_CS	I/O	SSP1_CS	I/O

IO Port Name	PKG 9x9	PKG 11x11	IO Bank	Mode4	DIR	Mode5	DIR	Mode6	DIR	Mode7	DIR
X_SSP1_DI	V	V		SSP1_DI	I	SSP1_DI	O	SSP1_DI	I	SSP1_DI	I
X_SSP1_DO	V	V		SSP1_DO	O	SSP1_DO	O	SSP1_DO	O	SSP1_DO	O
X_SSP1_DCX	V	V		SSP1_DCX	O	SSP1_DCX	O	SSP1_DCX	O	SSP1_DCX	O
X_PWM1	V	V		I2C0_DATA	I/O	PWM1	O	CORE_DBG_27	O	GPIO_27	I/O
X_DPI_PCLKO	V	V		DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O	DPI_PCLKO	O
X_DPI_VSO	V	V		DPI_VSO	O	DPI_VSO	O	DPI_VSO	O	DPI_VSO	O
X_DPI_HSO	V	V		DPI_HSO	O	DPI_HSO	O	DPI_HSO	O	DPI_HSO	O
X_DPI_DEO	V	V		DPI_DEO	O	DPI_DEO	O	DPI_DEO	O	DPI_DEO	O
X_DPI_DATAO[0]	V	V		DPI_DATAO[0]	O	DPI_DATAO[0]	O	DPI_DATAO[0]	O	DPI_DATAO[0]	O
X_DPI_DATAO[1]	V	V		DPI_DATAO[1]	O	DPI_DATAO[1]	O	DPI_DATAO[1]	O	DPI_DATAO[1]	O
X_DPI_DATAO[2]	V	V		DPI_DATAO[2]	O	DPI_DATAO[2]	O	DPI_DATAO[2]	O	DPI_DATAO[2]	O
X_DPI_DATAO[3]	V	V		DPI_DATAO[3]	O	DPI_DATAO[3]	O	DPI_DATAO[3]	O	DPI_DATAO[3]	O
X_DPI_DATAO[4]	V	V		DPI_DATAO[4]	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O	DPI_DATAO[4]	O
X_DPI_DATAO[5]	V	V		DPI_DATAO[5]	O	DPI_DATAO[5]	O	DPI_DATAO[5]	O	DPI_DATAO[5]	O
X_DPI_DATAO[6]	V	V		DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O	DPI_DATAO[6]	O
X_DPI_DATAO[7]	V	V		DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O	DPI_DATAO[7]	O
X_DPI_DATAO[8]	V	V		DPI_DATAO[8]	O	DPI_DATAO[8]	O	CORE_DBG_28	O	GPIO_28	I/O
X_DPI_DATAO[9]	V	V		DPI_DATAO[9]	O	DPI_DATAO[9]	O	CORE_DBG_29	O	GPIO_29	I/O
X_DPI_DATAO[10]	V	V		DPI_DATAO[10]	O	DPI_DATAO[10]	O	CORE_DBG_30	O	GPIO_30	I/O
X_DPI_DATAO[11]	V	V		DPI_DATAO[11]	O	DPI_DATAO[11]	O	CORE_DBG_31	O	GPIO_31	I/O
X_I2C2_CLK		V	Bank2 by IO	Reserve	I	MCU_JTAG_TMS	I	CORE_DBG_4	O	GPIO_4	I/O
X_I2C2_DATA		V		Reserve	I	MCU_JTAG_TCK	I	CORE_DBG_5	O	GPIO_5	I/O
X_DSP_TRSTN	V	V		I2C1_CLK	I/O	Reserve	O	CORE_DBG_10	O	GPIO_10	I/O
X_DSP_TDI	V	V		I2C1_DATA	I/O	Reserve	O	CORE_DBG_11	O	GPIO_11	I/O
X_DSP_TDO		V		I2C2_CLK	I/O	Reserve	O	CORE_DBG_12	O	GPIO_12	I/O
X_DSP_TMS		V		I2C2_DATA	I/O	Reserve	O	CORE_DBG_13	O	GPIO_13	I/O
X_DSP_TCK		V		Reserve	O	Reserve	O	CORE_DBG_14	O	GPIO_14	I/O
X_PWM0	V	V		I2C0_CLK	I/O	PWM0	O	CORE_DBG_26	O	GPIO_26	I/O
X_JTAG_TRSTN	V	V	Bank4 (3.3V)	SSP0_CS0	I/O	HSPI_CLK	I	CORE_DBG_6	O	GPIO_6	I/O
X_JTAG_TDI	V	V		SSP0_CS1	I	HSPI_CS	I	CORE_DBG_7	O	GPIO_7	I/O
X_JTAG_TMS	V	V		SSP0_DI	I	HSPI_DI	I	CORE_DBG_8	O	GPIO_8	I/O
X_JTAG_TCK	V	V		SSP0_DO	O	HSPI_DO	O	CORE_DBG_9	O	GPIO_9	I/O
X_SD1_D3	V	V		SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O	SD1_D3	I/O
X_SD1_D2	V	V		SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O	SD1_D2	I/O
X_SD1_D1	V	V		SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O	SD1_D1	I/O
X_SD1_D0	V	V		SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O	SD1_D0	I/O
X_SD1_CMD	V	V		SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O	SD1_CMD	I/O
X_SD1_CLK	V	V		SD1_CLK	O	SD1_CLK	O	SD1_CLK	O	SD1_CLK	O
X_SD0_D3	V	V		SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O	SD0_D3	I/O
X_SD0_D2	V	V		SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O	SD0_D2	I/O
X_SD0_D1	V	V		SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O	SD0_D1	I/O
X_SD0_D0	V	V		SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O	SD0_D0	I/O
X_SD0_CMD	V	V		SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O	SD0_CMD	I/O
X_SD0_CLK	V	V		SD0_CLK	O	SD0_CLK	O	SD0_CLK	O	SD0_CLK	O
X_SD0_CARD_PWN	V	V		SD0_CARD_PWREN	O	SD0_CARD_PWREN	O	CORE_DBG_23	O	GPIO_23	I/O
X_SD0_CARD_DET	V	V		SD0_CARD_DET	I	SD0_CARD_DET	I	CORE_DBG_24	O	GPIO_24	I/O
X_JTAG_TDO	V	V		SD0_W_PORT	I	SD0_W_PORT	I	CORE_DBG_25	O	GPIO_25	I/O

3.3 Signal Description

Table 4 - Signal description

Signal Name	Description
Boot setting	
X_OM	System mode setting 0: Normal mode 1: Test mode, don't used on normal operation
X_OSCL_SEL	Select SCU clock source. 0: 32.768KHz from OSC pad. 1: OSC 100KHz from internal OSC.
BK1_LS3V	IO bank1 voltage select. 0: V18. 1: V33
BK2_LS3V	IO bank2 voltage select. 0: V18. 1: V33
BOOT_IPL_SEL	Share with X_JTAG_TDO 0: Boot from SPI NOR (XIP mode) 1: Boot from ROM
BOOT_SPL_SEL[1:0]	Share with X_SSP1_DO, X_SSP0_DO 00: SPL is specified by UART 01: SPL is located in SPI NOR flash 10: SPL is located in SPI NAND flash 11: SPL is from USB.
HSPI_IF_ON	Share with X_UART0_TX 0: Normal. 1: Reserve, don't used on normal operation
Clock/Reset	
X_RESET_N	Chip full reset
X_WAK_BTN	Base domain for wake up trigger
X_OSCRTC_IO	32.768KHz crystal IO
X_OSCRTC_IN	32.768KHz crystal Input
X_OSC12M_IN	12.000MHz crystal IO
X_OSC12M_IO	12.000MHz crystal Input
Power switch control	
X_PSW_BAS	Base power domain enable. '1': enable, '0': disable
X_PSW_NOM	Normal power domain enable. '1': enable, '0': disable
X_PSW_UHO	USB2 power domain enable. '1': enable, '0': disable
X_PSW_UDR	USB3 power domain enable. '1': enable, '0': disable

Signal Name	Description
X_PSW_DCK	KGD power domain enable. ‘1’: enable, ‘0’: disable
X_PSW_NPU	NPU and DSP power domain enable. ‘1’: enable, ‘0’: disable
X_PSW_MRX	MIPI power domain enable. ‘1’: enable, ‘0’: disable
X_PSW_EXT	External power domain enable. ‘1’: enable, ‘0’: disable
USB 2.0/ USB3.0	
X_USB2_DP	USB2 DP signal
X_USB2_DM	USB2 DM signal
X_USB2_DRVVBUS	USB2 VBUS power enable
X_USB2_VBUS	USB2 VBUS power detect.
X_USB2_RREF	USB2 current source. It needs to connect the 4.7-kΩ ± 1% resistor
X_USB3_SSTXA	USB3 SSTXA signal, default connect to SSTX-
X_USB3_SSTXB	USB3 SSTXB signal, default connect to SSTX+
X_USB3_SSRXA	USB3 SSRXA signal, default connect to SSRX-
X_USB3_SSRXB	USB3 SSRXB signal, default connect to SSRX+
X_USB3_DP	USB3 DP signal
X_USB3_DM	USB3 DM signal
X_USB3_DRVVBUS	USB3 VBUS power enable
X_USB3_VBUS	USB3 VBUS power detect.
X_USB3_RREF	USB3 current source. It needs to connect the 4.7-kΩ ± 1% resistor
X_USB3_ID	USB3 ID pin. ‘0’: Host, ‘1’: Device
SPI flash	
SPI_CLK	Serial clock
SPI_CS_N	Chip select, active low
SPI_DI	Data input / IO0
SPI_DO	Data output / IO1
SPI_WP_N	IO2(for SPI flash quad-mode)
SPI_HOLD_N	IO3(for SPI flash quad-mode)
DPI output	
DPI_PCLKO	Pixel clock
DPI_VSO	Vertical sync
DPI_HSO	Horizontal sync
DPI_DEO	Data enable
DPI_DATAO[11:0]	Pixel data[11:0]
DPI input	
DPI_PCLKI	Pixel clock
DPI_VSI	Vertical sync
DPI_HSI	Horizontal sync
DPI_DEI	Data enable
DPI_DATAI[15:0]	Pixel data[15:0]

Signal Name	Description
MCU JTAG	
JTAG_TRSTN	JTAG reset
JTAG_TDI	JTAG data input
JTAG_TMS	JTAG mode select or SWDIO
JTAG_TCK	JTAG clock or SWCLK
JTAG_TDO	JTAG data out
DSP JTAG	
DSP_TRSTN	JTAG reset
DSP_TDI	JTAG data input
DSP_TDO	JTAG data output
DSP_TMS	JTAG mode select
DSP_TCK	JTAG clock
I2C Interface	
I2C0_CLK	I2C0 SCL, open drain
I2C0_DATA	I2C0 SDA, open drain
I2C1_CLK	I2C1 SCL, open drain
I2C1_DATA	I2C1 SDA, open drain
I2C2_CLK	I2C2 SCL, open drain
I2C2_DATA	I2C2 SDA, open drain
I2S clock	
MCLK	Master mode clock
Serial interface 0	
SSP0_CLK	Serial clock
SSP0_CS0	Chip select 0 @SSP and SPI mode, FS @ I2S mode
SSP0_CS1	Chip select 1 @SSP and SPI mode, not used @ I2S mode
SSP0_DI	Data input
SSP0_DO	Data output
Serial interface 1	
SSP1_CLK	Serial clock
SSP1_CS	Chip select @SSP and SPI mode, FS @ I2S mode
SSP1_DI	Data input
SSP1_DO	Data output
SSP1_DCX	Data/CMD flag
PWM	
PWM0	Pulse width modulation 0 output
PWM1	Pulse width modulation 1 output
UART	
UART0_TX	UART0 Data output
UART0_RX	UART0 Data input

Signal Name	Description
UART1_TX	UART1 Data output
UART1_RX	UART1 Data input
GPIO interface	
GPIO_*	Programmable general-purpose input/output
SD card interface	
SD0_CLK	Clock
SD0_CMD	Command
SD0_CARD_PWN	Card Power enable control
SD0_CARD_DET	Card detect
SD0_D[3:0]	Data[3:0]
SDIO interface	
SD1_CLK	Clock
SD1_CMD	Command
SD1_D[3:0]	Data[3:0]
DDR PHY/ KGD	
ZQ	DDR PHY ZQ, it needs to connect the 240 Ω ± 1% resistor to GND
X_DDR_ZQ	KGD ZQ, it needs to connect the 240 Ω ± 1% resistor to GND
ODT	KGD ODT signal, suggest connect the 1K Ω resistor to VCC120_DDR
VREF_CA	KGD VREF_CA
VREF_DQ	KGD VREF_DQ
X_DDR_ATO	DDR PHT test pin, please floating it.
X_DDR_DTO[1:0]	DDR PHT test pin, please floating it.
MIPI RX	
X_MPRX0_CKP	MIPI0 differential clock lane+
X_MPRX0_CKN	MIPI0 differential clock lane-
X_MPRX0_DP0	MIPI0 differential data lane 0+
X_MPRX0_DN0	MIPI0 differential data lane 0-
X_MPRX0_DP1	MIPI0 differential data lane 1+
X_MPRX0_DN1	MIPI0 differential data lane 1-
X_MPRX0_RBIAS	MIPI0 RBIAS, it must connect the 2k Ω resistor (±1%) to GND
X_MPRX1_CKP	MIPI1 differential clock lane+
X_MPRX1_CKN	MIPI1 differential clock lane-
X_MPRX1_DP0	MIPI1 differential data lane 0+
X_MPRX1_DN0	MIPI1 differential data lane 0-
X_MPRX1_DP1	MIPI1 differential data lane 1+
X_MPRX1_DN1	MIPI1 differential data lane 1-
X_MPRX1_RBIAS	MIPI1 RBIAS, it must connect the 2k Ω resistor (±1%) to GND

3.4 Power supply pin

- FCCSP 9x9 power supply ball assign

Table 5 - FCCSP 9x9 power supply ball assign

Pin name	Description	Pin no.	Power Domain
VCC09A_PLL0_6 VCC09A_PLL1 VCC09A_PLL4 VCC09A_PLL5	PLL power	F13 F9 J9 N10	X_PSW_BAS
VCC09A_RX_USB3	USB 3 RX power	D12	X_PSW_BAS
VCC09A_TX_USB3	USB 3 TX power	D10	X_PSW_BAS
VCC09K_PHY	DDR PHY digital power	K7, L7, P7, P8	X_PSW_BAS
VCC120_DDR	DDR PHY IO power	D2,E2,E3,G6,H6,J6,M6,M7,N6,N7,P3,P4,P5,P6	X_PSW_BAS
VDD2_CA_KGD12A	DDR PHY IO power	H1,H2,J1,J2,J3,J4	X_PSW_BAS
VCCK_BNU	BAS, NOR, USB2, USB3 core power	E10,E14,F10,F11,F14,G10,H10,J10,L15,M12,M13, M14	X_PSW_BAS
VCCK_NPU	DSP, NPU core power	F12,F15,G11,G12,G14,G15,H11,H12,H14,H15,J11, J13,J15,K11,K13,K15,L12,L14,M10,M11,N11,N12, N13,N14,E10,E14,F10,F11,F14,G10,H10,J10,L15, M12,M13,M14	X_PSW_NPU
VCCK_OSC12M	OSC core power	E11	Always on
VDD1_KGD18A	KGD core power	K1	X_PSW_BAS
VCC18A_DDR_PLL	DDR PHY PLL power	H8	X_PSW_BAS
VCC18A_TDC0	TDC power	K9	X_PSW_BAS
VCC18A_USB2	USB2 analog power	B6	X_PSW_BAS
VCC18A_USB3	USB3 analog power	B12	X_PSW_BAS
VCC18A_VQPS0_1	Efuse power	J17	X_PSW_BAS
VCC18IO_RTC	RTC power	C7	Always on
VCC18UD_BK	Pin mux I/O power	K17,L16,M15,N15,R11,R12	X_PSW_BAS
VCC18UD_USB	USB2,3 IO power	B8	X_PSW_BAS
VCC33A_USB2	USB2 analog power	D6	X_PSW_BAS
VCC33A_USB3	USB3 analog power	C10	X_PSW_BAS
VCC3IO_BK0_1	IO bank 0,1 power	G16,H16,J16,K16	X_PSW_BAS
VCC3IO_BK2	IO bank 2 power	P13	X_PSW_BAS
VCC3IO_BK3	IO bank 3 power	P14,P15	X_PSW_BAS
VCC3IO_BK4	IO bank 4 power	P10,P11	X_PSW_BAS
VCC3IO_USB	USB 2,3 IO power	A10	X_PSW_BAS
VREF_CA	KGD CA VREF	K2	X_PSW_BAS
VREF_DQ	KGD DQ VREF	F4	X_PSW_BAS
GND18A_TDC0	TDC Ground	L9	
GND	Ground	A1,A12,A15,A17,B3,B7,B15,C3,C4,C5,C8,C9,C11, C13,C14,D3,D4,D13,D14,E4,E5,E6,E7,E8,E9,E13, E15,F3,F5,F6,F7,F8,G3,G7,G8,G9,G13,H4,H5,H7, H13,J5,J7,J8,J12,J14,K3,K4,K8,K12,K14,L3,L4,L5,	

		L8,L10,L11,L13,M3,M4,M5,M8,N3,N4,N5,N9,P9, R5,R6,R14,R15,U1,U17	

◆ FCCSP 11x11 power supply ball assign

Table 6 - FCCSP 11x11 power supply ball assign

Pin name	Description	Pin no.	Power Domain
VCC09A_PLL0_6 VCC09A_PLL1 VCC09A_PLL2_3 VCC09A_PLL4 VCC09A_PLL5	PLL power	H13 H9 E13 L9 R10	X_PSW_BAS
VCC09A_RX_USB3	USB 3 RX power	E11	X_PSW_BAS
VCC09A_TX_USB3	USB 3 TX power	E10	X_PSW_BAS
VCC09K_PHY	DDR PHY digital power	M7,N7,T7,T8	X_PSW_BAS
VCC09A_MPRX0	MIPI0 PHY analog power	C13	X_PSW_BAS
VCC09A_MPRX1	MIPI1 PHY analog power	C16	X_PSW_BAS
VCC120_DDR	DDR PHY IO power	E3,F3,G3,H7,J7,K6,L6,R4,R5,T3,T4,T5,U3,U4,U5	X_PSW_BAS
VDD2_CA_KGD12A	DDR PHY IO power	H4,J4,K3,K4,L3,L4	X_PSW_BAS
VCCK_BNUM	BAS,NOR,USB2,USB3,MIPI core power	G10,G11,G14,H10,H14,J10,K10,L10,N15,P12,P13,P14	X_PSW_BAS
VCCK_NPU	DSP,NPU core power	H12,H15,J11,J12,J14,J15,K11,K12,K14,K15,L11,L13,L15,M11,M13,M15,N12,N14,P10,P11,R11,R12,R13,R14	X_PSW_NPU
VCCK_OSC12M	OSC core power	H11	Always on
VDD1_KGD18A	DDR core power 1.8V	K1	X_PSW_BAS
VCC12A_MPRX0	MIPI0 PHY reference voltage from LDO, need add 2.2uF on PCB.	C14	X_PSW_BAS
VCC12A_MPRX1	MIPI1 PHY reference voltage from LDO, need add 2.2uF on PCB.	C18	X_PSW_BAS
VCC18A_DDR_PLL	DDR PHY PLL analog power	K8	X_PSW_BAS
VCC18A_TDC0	TDC power	M9	X_PSW_BAS
VCC18A_USB2	USB2 analog power	E5	X_PSW_BAS
VCC18A_USB3	USB3 analog power	C10	X_PSW_BAS
VCC18A_VQPS0_1	Efuse power	L17	X_PSW_BAS
VCC18IO_RTC	RTC power	E7	Always on
VCC18UD_BK	Pin mux I/O power	M17,N16,P15,R15,U11,U12	X_PSW_BAS
VCC18UD_USB	USB2,3 IO power	C4	X_PSW_BAS
VCC18A_MPRX0	MIPI0 PHY analog power	C12	X_PSW_BAS
VCC18A_MPRX1	MIPI1 PHY analog power	A15	X_PSW_BAS
VCC33A_USB2	USB2 analog power	F6	X_PSW_BAS
VCC33A_USB3	USB3 analog power	C9	X_PSW_BAS
VCC3IO_BK0_1	IO bank 0,1 power	J16,K16,L16,M16	X_PSW_BAS

Pin name	Description	Pin no.	Power Domain
VCC3IO_BK2	IO bank 2 power	T13	X_PSW_BAS
VCC3IO_BK3	IO bank 3 power	T14,T15	X_PSW_BAS
VCC3IO_BK4	IO bank 4 power	T10,T11	X_PSW_BAS
VCC3IO_USB	USB 2,3 IO power	C5	X_PSW_BAS
VREF_CA	KGD CA VREF	J3	X_PSW_BAS
VREF_DQ	KGD DQ VREF	J6	X_PSW_BAS
GND18A_TDC0	TDC Ground	N9	
GND	Ground	A1,A4,A11,A19,A21,AA1,AA21,B11,B19,C3,C6,C7, C8,C11,C15,D19,E4,E6,E8,E9,E12,E14,E15,E16,E17,E19,F4,F5,F8,F9,F10,F12,F13,F14,F15,F16,F17,F19,G4,G5,G6,G7,G8,G9,G13,G15,G16,G17,G19,H5,H6,H8,H16,H17,H19,J8,J9,J13,J17,J19,K5,K7,K13,K17,K19,L5,L7,L8,L12,L14,L19,M5,M8,M12,M14,M19,N3,N4,N5,N6,N8,N10, N11,N13,N17,N19,P3,P4,P5,P6,P7,P8,P16,P17,P19,R3,R6,R7,R8,R9,R16,R17,R19,T6,T9,T16,T17,T19,U6,U7,U8,U9,U14,U15,U16,U17,U19,V3,V19,W3,W4,W5,W6,W7,W8,W9,W10,W11,W12,W13,W14,W15,W16,W17,W18,W19	

3.5 Ball map

Table 7 - FCCSP 9x9 ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	GND	X_PSW_UHO	X_RESET_N	X_USB2_DRVVBUS	X_USB2_DM	X_USB2_VBUS	X_OSC12M_IN	X_OSC12M_IO	X_USB3_ID	VCC3IO_USB	X_USB3_DM	GND	X_USB3_SSTXA	X_USB3_SSRXA	GND	X_MCLK	GND	A
B	X_OSCL_SEL	X_OM	GND	X_PSW_UDR	X_USB2_DP	VCC18A_USB2	GND	VCC18UD_USB	X_USB3_DRVVBUS	X_USB3_VBUS	X_USB3_DP	VCC18A_USB3	X_USB3_SSTXB	X_USB3_SSRXB	GND	X_SPI_CS_N	X_SPI_DI	B
C	X_OSCRTC_IO	X_PSW_NOM	GND	GND	GND	X_USB2_RREF	VCC18IO_RTC	GND	GND	VCC33A_USB3	GND	X_USB3_RREF	GND	GND	X_I2C0_DATA	X_SPI_WP_N	X_SPI_DO	C
D	X_OSCRTC_IN	VCC120_DDR	GND	GND		VCC33A_USB2				VCC09A_TX_USB3		VCC09A_RX_USB3	GND	GND	X_I2C0_CLK	X_SPI_CLK	X_SPI_HOLD_N	D
E	X_PSW_BAS	VCC120_DDR	VCC120_DDR	GND	GND	GND	GND	GND	GND	VCCK_BNU	VCCK_OSC12M		GND	VCCK_BNU	GND	X_SSP0_CS0	X_SSP0_CLK	E
F	X_PSW_EXT	X_WAK_BTN	GND	VREF_DQ	GND	GND	GND	GND	VCC09A_PLL1	VCCK_BNU	VCCK_BNU	VCCK_NPU	VCC09A_PLL0_6	VCCK_BNU	VCCK_NPU	X_SSP0_DI	X_SSP0_DO	F
G	X_PSW_NPU	X_PSW_DCK	GND	X_DDR_DTO[1]		VCC120_DDR	GND	GND	GND	VCCK_BNU	VCCK_NPU	VCCK_NPU	GND	VCCK_NPU	VCCK_NPU	VCC3IO_BK0_1	X_UART0_TX	G
H	VDD2_CA_KGD12A	VDD2_CA_KGD12A	X_DDR_ATO	GND	GND	VCC120_DDR	GND	VCC18A_DDR_PLL		VCCK_BNU	VCCK_NPU	VCCK_NPU	GND	VCCK_NPU	VCCK_NPU	VCC3IO_BK0_1	X_UART0_RX	H
J	VDD2_CA_KGD12A	VDD2_CA_KGD12A	VDD2_CA_KGD12A	VDD2_CA_KGD12A	GND	VCC120_DDR	GND	GND	VCC09A_PLL4	VCCK_BNU	VCCK_NPU	GND	VCCK_NPU	GND	VCCK_NPU	VCC3IO_BK0_1	VCC18A_VQPS0_1	J
K	VDD1_KGD18A	VREF_CA	GND	GND		X_DDR_DTO[0]	VCC09K_PHY	GND	VCC18A_TDC0		VCCK_NPU	GND	VCCK_NPU	GND	VCCK_NPU	VCC3IO_BK0_1	VCC18UD_BK	K
L	ZQ	ODT	GND	GND	GND	VCC120_DDR	VCC09K_PHY	GND	GND18A_TDC0	GND	GND	VCCK_NPU	GND	VCCK_NPU	VCCK_BNU	VCC18UD_BK	X_I2C1_CLK	L
M	X_DDR_ZQ	X_SD0_CARD_DET	GND	GND	GND	VCC120_DDR	VCC120_DDR	GND		VCCK_NPU	VCCK_NPU	VCCK_BNU	VCCK_BNU	VCCK_BNU	VCC18UD_BK	X_I2C1_DATA	X_SSP1_CLK	M
N	X_SD0_CARD_PWN	X_SD0_D1	GND	GND	GND	VCC120_DDR	VCC120_DDR		GND	VCC09A_PLL5	VCCK_NPU	VCCK_NPU	VCCK_NPU	VCCK_NPU	VCC18UD_BK	X_DPI_PCLKO	X_SSP1_DO	N
P	X_SD0_D0	X_SD0_CLK	VCC120_DDR	VCC120_DDR	VCC120_DDR	VCC120_DDR	VCC09K_PHY	VCC09K_PHY	GND	VCC3IO_BK4	VCC3IO_BK4		VCC3IO_BK2	VCC3IO_BK3	VCC3IO_BK3	X_DPI_DEO	X_SSP1_DI	P
R	X_SD0_CMD	X_SD0_D3			GND	GND					VCC18UD_BK	VCC18UD_BK		GND	GND	X_DPI_HSO	X_SSP1_CS	R
T	X_SD0_D2	X_SD1_D1	X_SD1_CLK	X_SD1_D3	X_BK2_LS3V	X_BK1_LS3V	X_JTAG_TRSTN	X_DSP_TRSTN	X_PWM0	X_DSP_TDI	X_DPI_DATAO[8]	X_DPI_DATAO[10]	X_DPI_DATAO[6]	X_DPI_DATAO[7]	X_PWM1	X_DPI_DATAO[4]	X_SSP1_DCX	T
U	GND	X_SD1_D0	X_SD1_CMD	X_SD1_D2	X_JTAG_TMS	X_JTAG_TDI	X_JTAG_TDO	X_JTAG_TCK	X_DPI_DATAO[11]	X_DPI_DATAO[9]	X_DPI_DATAO[3]	X_DPI_DATAO[5]	X_DPI_DATAO[2]	X_DPI_DATAO[1]	X_DPI_DATAO[0]	X_DPI_VSO	GND	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Table 8 - FCCSP 11x11 ball map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	GND	X_PSW_UDR	X_USB2_DM	GND	X_OSC12M_IN	X_OSC12M_IO	X_USB3_VBUS	X_USB3_DM	X_USB3_SSTXA	X_USB3_SSRXA	GND	X_MPRX0_CKP	X_MPRX0_DP1	X_MPRX0_DP0	VCC18A_MPRX1	X_MPRX1_CKP	X_MPRX1_DP1	X_MPRX1_DP0	GND	X_DPI_PCLKI	GND	A
B	X_RESET_N	X_PSW_UHO	X_USB2_DP	X_USB2_DRVVBUS	X_USB2_VBUS	X_USB3_DRVVBUS	X_USB3_ID	X_USB3_DP	X_USB3_SSTXB	X_USB3_SSRXB	GND	X_MPRX0_CKN	X_MPRX0_DN1	X_MPRX0_DN0	X_MPRX0_RBIAS	X_MPRX1_CKN	X_MPRX1_DN1	X_MPRX1_DN0	GND	X_DPI_DATAI[1]	X_DPI_HSI	B
C	X_OM	X_PSW_MRX	GND	VCC18UD_USB	VCC3IO_USB	GND	GND	GND	VCC33A_USB3	VCC18A_USB3	GND	VCC18A_MPRX0	VCC09A_MPRX0	VCC12A_MPRX0	GND	VCC09A_MPRX1	X_MPRX1_RBIAS	VCC12A_MPRX1	X_DPI_VSI	X_DPI_DEI	X_DPI_DATAI[0]	C
D	X_OSCL_SEL	X_PSW_NOM	X_USB2_RREF					X_USB3_RREF											GND	X_DPI_DATAI[2]	X_DPI_DATAI[3]	D
E	X_OSCRTC_IO	X_OSCRTC_IN	VCC120_DDR	GND	VCC18A_USB2	GND	VCC18IO_RTC	GND	GND	VCC09A_TX_USB3	VCC09A_RX_USB3	GND	VCC09A_PLL2_3	GND	GND	GND	GND		GND	X_DPI_DATAI[5]	X_DPI_DATAI[4]	E
F	X_PSW_BAS	X_WAK_BTN	VCC120_DDR	GND	GND	VCC33A_USB2		GND	GND	GND		GND	GND	GND	GND	GND	GND		GND	X_DPI_DATAI[6]	X_DPI_DATAI[7]	F
G	X_PSW_EXT	X_PSW_DCK	VCC120_DDR	GND	GND	GND	GND	GND	GND	VCCK_BNUM	VCCK_BNUM		GND	VCCK_BNUM	GND	GND	GND		GND	X_DPI_DATAI[9]	X_DPI_DATAI[8]	G
H	X_PSW_NPU	X_DDR_ATO	X_DDR_DTO[1]	VDD2_CA_KGD12A	GND	GND	VCC120_DDR	GND	VCC09A_PLL1	VCCK_BNUM	VCCK_OSC12M	VCCK_NPU	VCC09A_PLL0_6	VCCK_BNUM	VCCK_NPU	GND	GND		GND	X_DPI_DATAI[11]	X_DPI_DATAI[10]	H
J	ODT	X_DDR_DTO[0]	VREF_CA	VDD2_CA_KGD12A		VREF_DQ	VCC120_DDR	GND	GND	VCCK_BNUM	VCCK_NPU	VCCK_NPU	GND	VCCK_NPU	VCCK_NPU	VCC3IO_BK0_1	GND		GND	X_DPI_DATAI[13]	X_DPI_DATAI[12]	J
K	VDD1_KGD18A	ZQ	VDD2_CA_KGD12A	VDD2_CA_KGD12A	GND	VCC120_DDR	GND	VCC18A_DDR_PLL		VCCK_BNUM	VCCK_NPU	VCCK_NPU	GND	VCCK_NPU	VCCK_NPU	VCC3IO_BK0_1	GND		GND	X_DPI_DATAI[15]	X_DPI_DATAI[14]	K
L	X_DDR_ZQ	X_BK2_LS3V	VDD2_CA_KGD12A	VDD2_CA_KGD12A	GND	VCC120_DDR	GND	GND	VCC09A_PLL4	VCCK_BNUM	VCCK_NPU	GND	VCCK_NPU	GND	VCCK_NPU	VCC3IO_BK0_1	VCC18A_VQPS0_1		GND	X_I2C0_DATA	X_MCLK	L
M	X_JTAG_TDO	X_BK1_LS3V			GND		VCC09K_PHY	GND	VCC18A_TDC0		VCCK_NPU	GND	VCCK_NPU	GND	VCCK_NPU	VCC3IO_BK0_1	VCC18UD_BK		GND	X_I2C0_CLK	X_SPI_CS_N	M
N	X_SD0_CARD_PWN	X_SD0_CARD_DET	GND	GND	GND	GND	VCC09K_PHY	GND	GND18A_TDC0	GND	GND	VCCK_NPU	GND	VCCK_NPU	VCCK_BNUM	VCC18UD_BK	GND		GND	X_SPI_DI	X_SPI_WP_N	N
P	X_SD0_D1	X_SD0_D0	GND	GND	GND	GND	GND	GND		VCCK_NPU	VCCK_NPU	VCCK_BNUM	VCCK_BNUM	VCCK_BNUM	VCC18UD_BK	GND	GND		GND	X_SPI_DO	X_SPI_CLK	P
R	X_SD0_CLK	X_SD0_CMD	GND	VCC120_DDR	VCC120_DDR	GND	GND	GND	GND	VCC09A_PLL5	VCCK_NPU	VCCK_NPU	VCCK_NPU	VCCK_NPU	VCC18UD_BK	GND	GND		GND	X_SPI_HOLD_N	X_SSP0_CLK	R
T	X_SD0_D3	X_SD0_D2	VCC120_DDR	VCC120_DDR	VCC120_DDR	GND	VCC09K_PHY	VCC09K_PHY	GND	VCC3IO_BK4	VCC3IO_BK4		VCC3IO_BK2	VCC3IO_BK3	VCC3IO_BK3	GND	GND		GND	X_SSP0_CS0	X_SSP0_DO	T
U	X_SD1_D1	X_SD1_D0	VCC120_DDR	VCC120_DDR	VCC120_DDR	GND	GND	GND	GND		VCC18UD_BK	VCC18UD_BK		GND	GND	GND	GND		GND	X_SSP0_DI	X_UART0_RX	U
V	X_SD1_CLK	X_SD1_CMD	GND																GND	X_UART0_TX	X_SSP0_CS1	V
W	X_SD1_D3	X_SD1_D2	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	X_TRACE_CLK	X_TRACE_DATA[0]	W
Y	X_JTAG_TMS	X_JTAG_TDI	X_DSP_TCK	X_DSP_TDO	X_DSP_TRSTN	X_DPI_DATAO[11]	X_DPI_DATAO[8]	X_DPI_DATAO[10]	X_DPI_DATAO[3]	X_DPI_DATAO[5]	X_DPI_DATAO[4]	X_DPI_DATAO[1]	X_DPI_VSO	X_DPI_PCLKO	X_SSP1_DCX	X_SSP1_DI	X_SSP1_CLK	X_I2C1_DATA	X_UART1_RI	X_TRACE_DATA[2]	X_TRACE_DATA[1]	Y
AA	GND	X_JTAG_TCK	X_JTAG_TRSTN	X_PWM0	X_DSP_TMS	X_DSP_TDI	X_I2C2_DATA	X_I2C2_CLK	X_DPI_DATAO[9]	X_DPI_DATAO[6]	X_DPI_DATAO[7]	X_DPI_DATAO[2]	X_DPI_DATAO[0]	X_DPI_DEO	X_DPI_HSO	X_PWM1	X_SSP1_CS	X_SSP1_DO	X_I2C1_CLK	X_TRACE_DATA[3]	GND	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

4. Power Mode

4.1 Introduction

In order to provide power efficient solution, there are four power planes in RTC, CPU, DSP & NPU, DDR.

4.2 Power mode

4.2.1 RTC mode

Only RTC power plane is active in this mode.

4.2.2 Default mode

This mode is triggered by wakeup signal. PSW_CPU will be active to enable PMIC (on board) to power to CPU power plane. Therefore, RTC and CPU power planes are active in this mode.

4.2.3 Full function mode

All the power planes are active to support full functions in this mode.

4.2.4 Retention mode

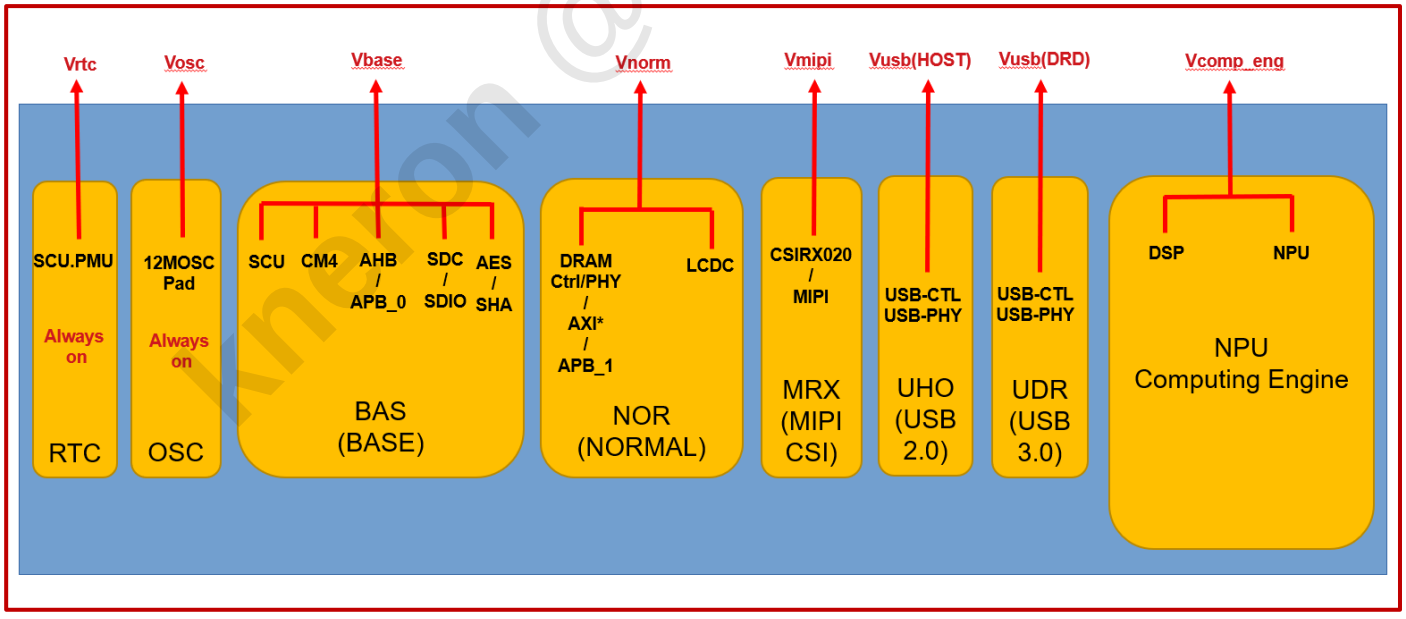
Enter this mode by turn off the power of DSP& NPU power plane from Full function mode. RTC, CPU and DDR power planes are active in this mode.

4.2.5 Deep retention mode

In this mode, DDR keeps self-refresh state to keep the data in DDR. RTC and DDR are active in this mode.

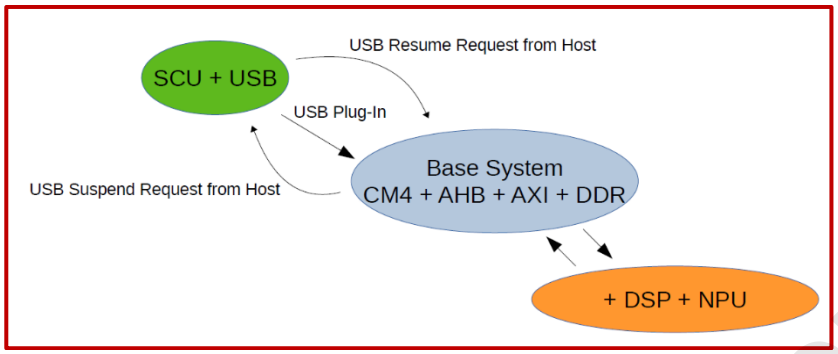
4.2.6 Power Domain

Figure 4 - Power domain



4.2.7 Power switch (on board) diagram

Figure 5 - Power switch diagram



5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 9 - Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Supply Core Voltage	V09	-0.5	1.26	V
Supply IO Voltage @ V33=3.3V	V33	-0.5	4.6	V
Supply IO Voltage @ V33 =1.8V	V33	-0.5	2.8	V
IO Signal Voltage @ V33 =3.3V	VIO	-0.5	4.6	V
IO Signal Voltage @ V33 =1.8V	VIO	-0.5	2.8	V
ESD (human body mode)	ESD-HBM		±1	KV
ESD (machine mode)	ESD-MM		±30	V
Latch-Up			±100	mA
Storage Temperature	Tstorage	-40	150	℃
Operation Temperature	Toperate	0	70	℃
Junction Temperature	Tjunction	-40	125	℃

[1] The voltage depends on different power group

* Permanent device damage may occur if the absolute maximum ratings are exceeded

5.2 Recommended operating conditions

Table 10 - Recommended operating conditions

Power pin	Description	Min.	Typ.	Max.	Unit
VCC33A_USB2 VCC33A_USB3 VCC3IO_BK0_1 VCC3IO_BK2 VCC3IO_BK3 VCC3IO_BK4 VCC3IO_USB	IO(digital IO, USB) power supply	3.135	3.3	3.465	V
VCC18A_DDR_PLL VCC18A_TDC0 VCC18A_USB2 VCC18A_USB3 VCC18A_VQPS0_1 VCC18IO_RTC VCC18UD_BK VCC18UD_USB VDD1_KGD18A	Efuse, USB and DDR power supply	1.71	1.8	1.89	V
VDD2_CA_KGD12A VCC120_DDR	DDR PHY power supply	1.2	1.25	1.3	V
VCC09A_PLL0_6 VCC09A_PLL1 VCC09A_PLL4 VCC09A_PLL5 VCC09K_PHY VCC09A_TX_USB3 VCC09A_RX_USB3 VCCK_BNU VCCK_NPU VCCK_OSC12M	PLL, core and USB power supply	0.9	0.945	0.99	V

5.3 DC electrical characteristics

Table 11 - DC electrical characteristics

Symbol	Description	Note	Min.	Typ.	Max.	Unit
V33	3.3V I/O and RTL-power domain power supply	VCC33A_USB2 VCC33A_USB3 VCC3IO_BK0_1 VCC3IO_BK2 VCC3IO_BK3 VCC3IO_BK4 VCC3IO_USB	3.135	3.3	3.465	V
T_j	Operating junction temperature	Tjunction	-40	25	125	°C
V_{Il}	Input low voltage @V33=3.3V	LVTTL	0.8	1.1		V
V_{Ih}	Input high voltage @V33=3.3V	LVTTL		1.58	2.0	V
V_{t-}	Schmitt-trigger negative-to threshold voltage @V33=3.3V	LVTTL	0.8	1.1		V
V_{t+}	Schmitt-trigger positive-to-threshold voltage @V33=3.3V	LVTTL		1.58	2.0	V
V_{Ol}	Output low voltage @V33=3.3V	I_{Ol} = 2mA~8mA			0.4	V
V_{Oh}	Output high voltage @V33=3.3V	I_{Oh} = 2mA~8mA	2.4			V
R_{pu}	Input pull-up resistance	V_{in} = 0V	20	40	100	KΩ
R_{pd}	Input pull-down resistance	V_{in} = V33	20	40	100	KΩ
I_{in}	Input leakage current	V_{in} = V33 or 0V		±1	±10	μA
I_{oz}	Tri-state put leakage current	-		±1	±10	μA

5.4 USB electrical characteristics

Table 12 - USB 3.2 Gen1 Electrical Characteristics of Transmitter

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
UI	Unit interval	-	199.94	200	200.06	ps
$V_{TX-DIFF-PP}$	Differential peak-to-peak TX voltage swing	2 * |V_{TXP} - V_{TXN}|, measured at the TX near end	800	-	1200	mV
$V_{TX-DIFF-PP\_LOW}$	Low-power differential peak-to-peak TX voltage swing	2 * |V_{TXP} - V_{TXN}|, measured at the TX near end	400	-	1200	mV
$V_{TX-DE-RATIO}$	TX de-emphasis level	-	3.0	-	4.0	dB
$R_{TX-DIFF-DC}$	DC differential impedance	-	72	-	120	Ω
$C_{AC-COUPLING}$	AC coupling capacitor	-	75	-	200	nF
$T_{TX-DJ-FAR}$	Far-end TX deterministic jitter	• Deterministic jitter assuming only the dual-Dirac distribution • Measured at TP1 and after receiver equalization function	-	-	0.43	UI
$T_{TX-RJ-FAR}$	Far-end TX random jitter	Measured at the TP1 and after receiver equalization function by using the CP1 pattern at 10^{-12} BER	-	-	0.23	UI
$T_{TX-TJ-FAR}$	Far-end TX total jitter	Measured at the TP1 and after receiver equalization (TJ = DJ + RJ)	-	-	0.66	UI
V_{TDR}	The voltage change allowed during the receiver detection	Total amount of the voltage change during TX-Detect-RX	-	-	600	mV

Table 13 - USB 3.2 Gen1 Parameters of Normative Spread Spectrum Clocking (SSC)

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
$T_{SSC-MOD-RATE}$	Modulation rate	-	30	-	33	kHz
$T_{SSC-FREQ-DEVIATION}$	SSC deviation	-	+0/-4000	-	+0/-5000	ppm
$T_{SSC-SLEW-RATE}$	SSC slew rate	-	-	-	10	ms/s

Table 14 - USB 3.2 Gen1 Electrical Characteristics of LFPS

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{Period}	Period of the LFPS signal	-	20	-	100	ns
$V_{CM-AC-LFPS}$	AC common-mode voltage of the LFPS signal	-	-	-	100	mV
$V_{TX-DIFF-PP-LFPS}$	Differential peak-to-peak LFPS voltage swing	$2 * \|V_{TXP} - V_{TXN}\|$	800	-	1200	mV
$V_{TX-DIFF-PP-LFPS-LP}$	Low-power differential peak-to-peak LFPS voltage swing	$2 * \|V_{TXP} - V_{TXN}\|$	400	-	600	mV
$T_{RISE-FALL-2080}$	Rise/Fall time of the LFPS signal	-	-	-	4.0	ns
Duty cycle	Duty cycle of the LFPS signal	-	40	-	60	%

Table 15 - USB 3.2 Gen1 Electrical Characteristics of Receivers

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
UI	Unit interval	-	199.94	200	200.06	ps
R_{RX-DC}	Receiver common-mode impedance	-	18	-	30	Ω
$R_{RX-DIFF-DC}$	Receiver DC differential impedance	-	72	-	120	Ω
$V_{RX-LFPSDET-DIFF-PP}$	LFPS detect threshold	-	100	-	300	mV

Table 16 - USB 3.2 Gen1 Input Jitter Requirements for Testing RX Tolerance

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
F1	Tolerance corner	-	-	4.9	-	MHz
J_{RJ}	Random jitter	-	-	0.0121	-	UI rms
J_{RJ_P-P}	Random jitter peak-to-peak at 10^{-12}	-	-	0.17	-	UI p-p
J_{PJ_500KHZ}	Sinusoidal jitter	-	-	2.0	-	UI p-p
J_{PJ_1MHZ}	Sinusoidal jitter	-	-	1.0	-	UI p-p
J_{PJ_2MHZ}	Sinusoidal jitter	-	-	0.5	-	UI p-p
J_{PJ_F1}	Sinusoidal jitter	-	-	0.2	-	UI p-p
J_{PJ_50MHZ}	Sinusoidal jitter	-	-	0.2	-	UI p-p

Note: SSC should be added to the testing equipment at all time.

Table 17 - USB 2.0 Transceiver DC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Input levels for High-Speed						
V_{HSDIFF}	High-Speed differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$ Measured at the connection as an application circuit	300	-	-	mV
V_{HSCM}	High-Speed data signaling common-mode voltage range	-	-50	-	500	mV
V_{HSSQ}	High-Speed squelch detection threshold	Squelch is detected.	-	-	100	mV
		Squelch is not detected.	200	-	-	mV
V_{HSDSC}	High-Speed disconnection detection threshold	Disconnection is detected.	625	-	-	mV
		Disconnection is not detected.	-	-	525	mV
Output levels for High-Speed						
V_{HSOI}	High-Speed idle-level output voltage (Differential)	-	-20	-	20	mV
V_{HSOL}	High-Speed low-level output voltage (Differential)	-	-20	-	20	mV
V_{HSOH} [7]	High-Speed high-level output voltage (Differential)	-	360	400	440	mV
V_{CHIRPJ}	Chirp-J output voltage (Differential voltage)	-	700	-	1100	mV
V_{CHIRPK}	Chirp-K output voltage (Differential voltage)	-	-900	-	-500	mV
$I_{DP/DM}$	Allowable output current of DP/DM lines	When the termination is 45 Ω ±10%	14.55	17.78	21.79	mA
Terminations for High-Speed						
Z_{HSDRV}	Driver output resistance	Equivalent resistance used for the internal chip	40.5	45	49.5	Ω
Z_{HSTERM}	Differential impedance	-	76.5	90	103.5	Ω

[7] The driven lines of High-Speed Test_J and Test_K are removed as certification requirements in January 2010.

Table 18 - USB 2.0 Transceiver AC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics (High-Speed mode)						
T_{HSDRAT}	High-Speed TX data rate	-	479.76	-	480.24	Mbps
T_{HSDRAT}	High-Speed RX data rate	-	479.76	-	480.24	Mbps
t_{HSR} [8]	High-Speed differential rise time	10% ~ 90%	100	-	-	ps
t_{HSF} [8]	High-Speed differential fall time	10% ~ 90%	100	-	-	ps
Driver timing (High-Speed mode)						
-	Driver waveform requirement	Please refer to the eye pattern of template 1.	Please follow template 1 in the USB 2.0 specification.			
Receiver timing (High-Speed mode, Template 4, USB 2.0 specification)						
-	Data source jitter and receiver jitter tolerance	Please refer to the eye pattern of template 4.	Please follow template 4 in the USB 2.0 specification.			

Table 19 - USB 1.1 Transceiver DC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Input levels for Low-/Full-Speed						
V_{IH}	High-level input voltage	Driven	2.0	-	-	V
V_{IHZ}	High-level input voltage	Floating	2.7	-	3.6	V
V_{IL}	Low-level input voltage	-	-	-	0.8	V
V_{DI}	Differential input sensitivity	$\|V_{I(DP)} - V_{I(DM)}\|$	0.2	-	-	V
V_{CM}	Differential common-mode voltage	Including the V_{DI} range	0.8	-	2.5	V
Input levels for Single-ended receiver						
V_{SE1}	Single-ended receiver threshold	-	0.8	-	2.0	V
Output levels for Full-Speed/Low-Speed						
V_{OL}	Low-level output voltage	-	0	-	0.3	V
V_{OH}	High-level output voltage	-	2.8	-	3.6	V
Terminations						
RPU1	Pull-up resistor during idle	Equivalent resistance used for the internal chip	900	-	1575	Ω
RPU2	Pull-up resistor during transmitting	Equivalent resistance used for the internal chip	1425	-	3090	Ω
RPD	Pull-down resistance	Equivalent resistance used for the internal chip	14.25	-	24.80	kΩ

[8] USB-IF relaxes the rise and fall time edge values of 300 ps (2133 V/µs) and 100 ps (6400 V/µs) for High-Speed signaling, and no waivers should be granted for edge rates faster than 100 ps.

Table 20 - USB 1.1 Transceiver AC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
Driver characteristics (Full-Speed mode)						
$T_{FDRATHS}$	Full-Speed TX data rate	-	11.994	-	12.006	Mbps
T_{FDRATE}	Full-Speed RX data rate	-	11.970	-	12.030	Mbps
t_{FR} [9]	Rise time	C_L = 50 pF 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	4.0	-	20	ns
t_{FF} [9]	Fall time	C_L = 50 pF 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	4.0	-	20	ns
Driver characteristics (Low-Speed mode)						
$T_{LDRATHS}$	Low-Speed TX data rate	-	1.49925	-	1.50075	Mbps
T_{LDRATE}	Low-Speed RX data rate	-	1.47750	-	1.52250	Mbps
t_{LR} [9]	Rise time	C_L = 200 pF ~ 600 pF 10% ~ 90% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
t_{LF} [9]	Fall time	C_L = 200 pF ~ 600 pF 90% ~ 10% of $\|V_{OH} - V_{OL}\|$	75	-	300	ns
Driving timing (Full-Speed mode)						
	propagation delay (VI, FSE0, OE to DP, DM)	For the detailed descriptions of VI, FSE0, and OE, please refer to the USB 1.1 specification.	-	-	15	ns
T_{FDEOP}	Source jitter from differential transitions to SE0 transition	-	-2.0	-	5.0	ns
T_{JR1}	Receiver jitter	To the next transition	-18.5	-	18.5	ns
T_{JR2}	Receiver jitter	For the paired transition	-9.0	-	9.0	ns
T_{FEOPT}	Source SE0 interval of EOP	-	160	-	175	ns
T_{FEOPR}	Receiver SE0 interval of EOP	-	82	-	-	ns
T_{FST}	Width of the SE0 interval during differential transition	-	-	-	14	ns
Driving timing (Low-Speed mode)						
T_{LDEOP}	Source jitter from differential transition to SE0 transition	-	-40	-	100	ns
T_{JR1}	Receiver jitter	To next transition	-75	-	75	ns
T_{JR2}	Receiver jitter	For the paired transition	-45	-	45	ns
T_{LEOPT}	Source SE0 interval of EOP	-	1.25	-	1.5	µs
T_{LEOPR}	Receiver SE0 interval of EOP	-	670	-	-	ns

[9] This measurement continues to be informational for FS and LS. However, this measurement is required for HS.

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_{LST}	Width of the SE0 interval during differential transition	-	-	-	210	ns
Not specified: Low-Speed delay time is dominated by slower t_{LR} or t_{LR}.						
Receiver timing (Full-Speed mode)						
$t_{PLH(rcv)}$ $t_{PHL(rcv)}$	Receiver propagation delay (DP; DM to RX_RCV)	For the detailed descriptions of RCV, please refer to the USB 1.1 specification.	-	-	18	ns
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to RX_DP, RX_DM)	-	-	-	18	ns

5.5 MIPI electrical characteristics

Table 21 - MIPI DC Electrical Characteristics of HS Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
$V_{CMRX(DC)}$	Common-mode voltage in the HS receive mode	70	-	330	mV	1, 2
V_{IDTH}	Differential input high threshold voltage	-	-	40	mV	-
V_{IDTL}	Differential input low threshold voltage	-40	-	-	mV	-
V_{IHHS}	Single-ended input high voltage	-	-	460	mV	1
V_{ILHS}	Single-ended input low voltage	-40	-	-	-	1
$V_{TERM-EN}$	Single-ended threshold voltage for HS termination enable	-	-	450	mV	-
Z_{ID}	Differential input impedance	80	100	125	Ω	-

Notes:

1. The values listed exclude the possible additional RF interference of 100-mV peak sine wave beyond 450 MHz.
2. The values listed include the ground difference of 50 mV between the transmitter and receiver as well as the static common-mode level tolerance, and variations below 450 MHz.

Table 22 - MIPI AC Electrical Characteristics of HS Receiver

Parameter	Description	Min	Nom	Max	Units	Note
$\Delta V_{CMRX(HF)}$	Common-mode interference beyond 450 MHz	-	-	100	mV	2
$\Delta V_{CMRX(LF)}$	Common-mode interference beyond 50 MHz ~ 450 MHz	-50	-	50	mV	1
C_{CM}	Common-mode termination	-	-	60	pF	3

Notes:

1. The values listed exclude the "static" ground shift of 50 mV.
2. $\Delta V_{CMRX(HF)}$ is the peak amplitude of a sine wave superimposed on the receiver inputs.
3. For higher bit rate, a 14-pF capacitor is needed to meet the common-mode return loss specification.

Table 23 - MIPI DC Electrical Characteristics of LP Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
V_{IH}	Logic 1 input voltage	740	-	-	mV	-
V_{IL}	Logic 0 input voltage is not at the ULP state.	-	-	550	mV	-
$V_{IL-ULPS}$	Logic 0 input voltage is at the ULP state.	-	-	300	mV	-
V_{HYST}	Input hysteresis	25	-	-	mV	-

Table 24 - MIPI AC Electrical Characteristics of LP Receiver

Parameter	Description	Min.	Typ.	Max.	Unit	Note
e_{SPIKE}	Input pulse rejection	-	-	300	Vps	1, 2, 3
T_{MIN-RX}	Minimum pulse width response	20	-	-	ns	4
V_{INT}	Peak interference amplitude	-	-	200	mV	-
f_{INT}	Interference frequency	450	-	-	MHz	-

Notes:

1. Time-voltage integration of a spike will be above V_{IL} at the LP-0 state or below V_{IH} at the LP-1 state.
2. An impulse of less than this value will not change the receiver state.
3. In addition to the required glitch rejection, implementers must ensure the rejection of known RF interferers.
4. An input pulse of greater than this value must toggle the output

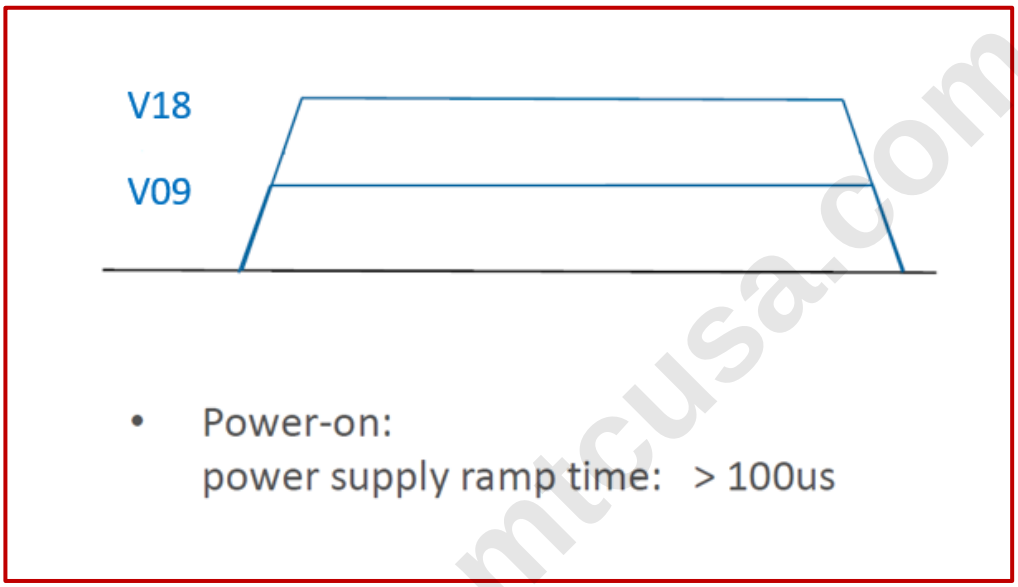
5.6 Power on/off sequence

Always-on Power domain

Table 25 - Always-on power list

Symbol	Power
V18	VCC18IO_RTC
V09	VCCK_OSC12M

Figure 6 - Always-on power on sequence



BNU Power domain

Table 26 - X_PSW_BAS power list

Symbol	Power
V33	VCC3IO_USB
	VCC33A_USB3
	VCC33A_USB2
	VCC3IO_BK4
V33 / V18	VCC3IO_BK0_1
	VCC3IO_BK2
	VCC3IO_BK3
V18	VCC18UD_USB
	VCC18UD_BK
	VCC18A_VQPS0_1
	VCC18A_USB3
	VCC18A_USB2
	VCC18A_TDC0
	VCC18A_DDR_PLL
	VCC18A_MPRX0
	VCC18A_MPRX1
	VDD1_KGD18A
V12	VCC120_DDR
	VDD2_CA_KGD12A
V09	VCC09K_PHY
	VCC09A_TX_USB3
	VCC09A_RX_USB3
	VCC09A_PLL5
	VCC09A_PLL4
	VCC09A_PLL1
	VCC09A_PLL0_6
	VCCK_BNUM
	VCC09A_MPRX0
	VCC09A_MPRX1

Figure 7 - BNU domain power supply ramp time requirement

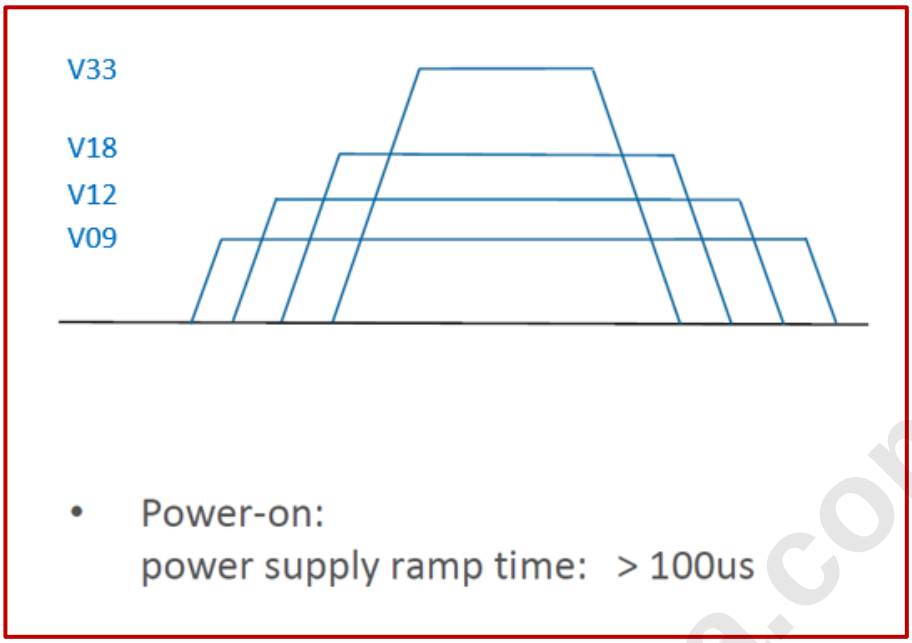
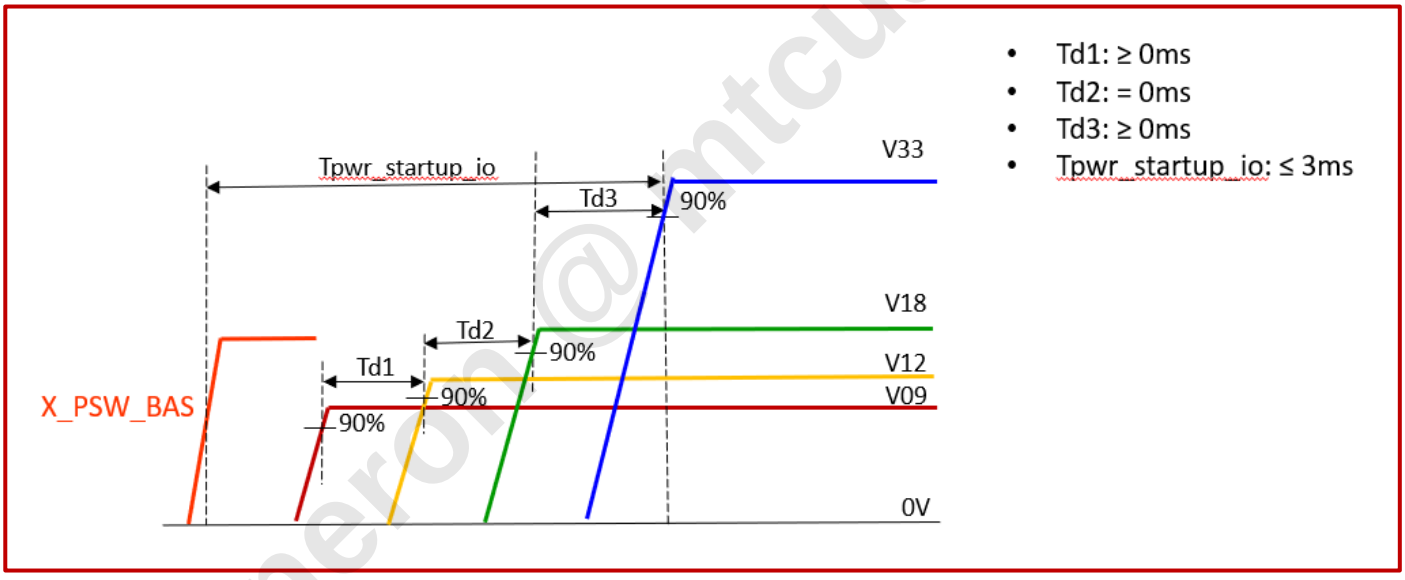


Figure 8 - BNU domain power up sequence requirement

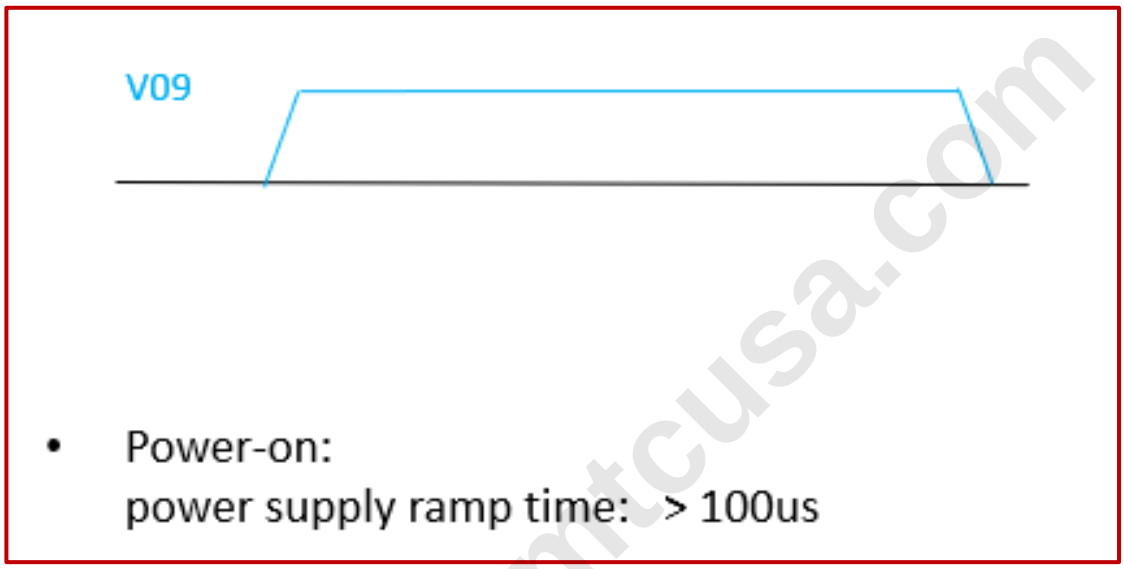


NPU power domain

Table 27 - NPU power domain list

Symbol	Power
V09	VCCK_NPU

Figure 9 - NPU power supply ramp time



5.6 Reset sequence

Figure 10 - Reset sequence

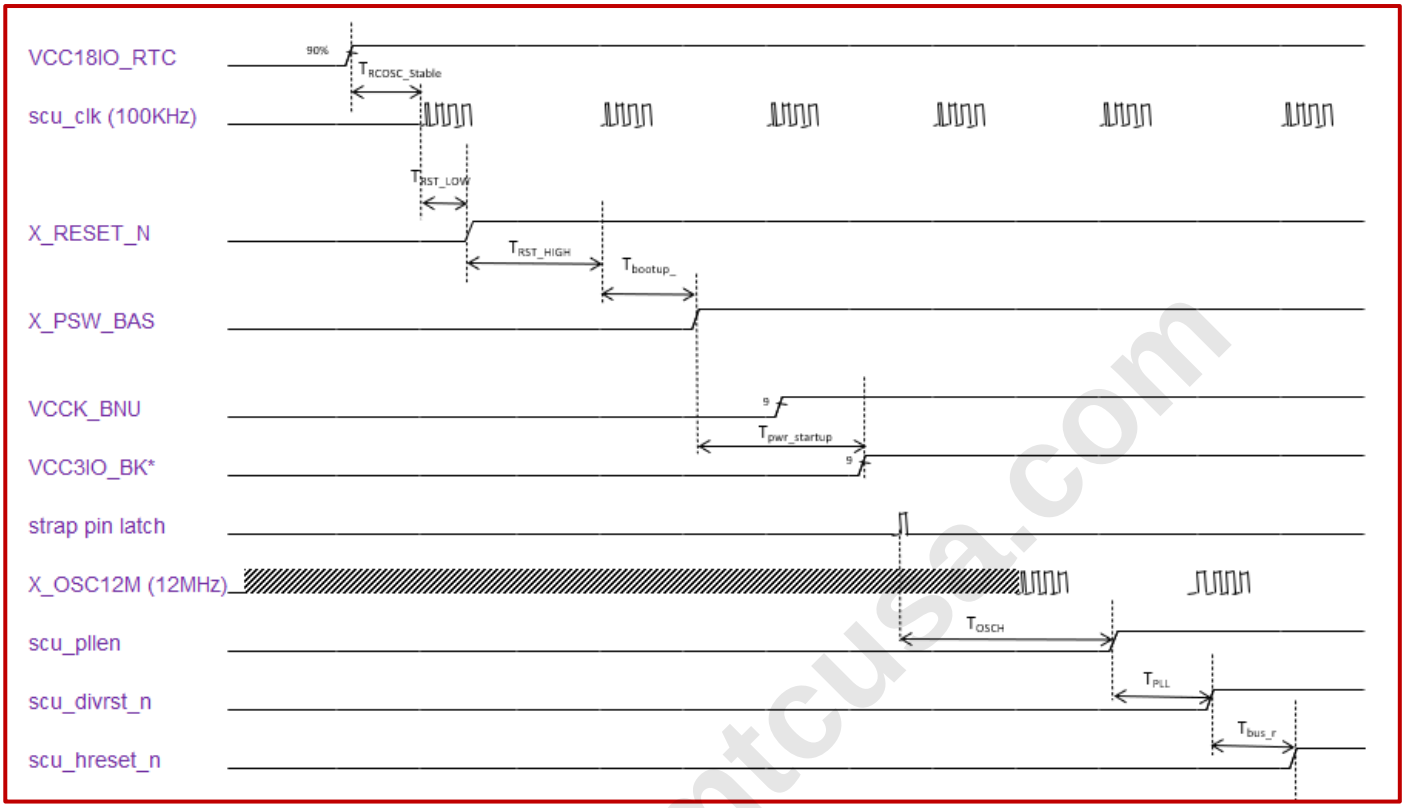


Table 28 - Reset sequence timing.

Symbol	Description	Min	Typ	Max	Units	Comment
T_{RCOSC_stable}	RCOSC stable time		110		us	
T_{RST_LOW}	Hardware reset low duration	67			us	It needs to keep low: Three cycles of scu_clk to make sure the reset event for de-glitch circuit.
T_{RST_HIGH}	Hardware reset high duration	715			us	It needs to keep high: At least thirty-two cycles of scu_clk to release the reset for the de-bounce circuit.
T_{bootup_en}	Bootup enable time		160		us	
$T_{pwr\_startup\_io}$	Power switch enable to IO power ready			3	ms	
T_{OSCH}	12MHz Crystal pad stable time		10		ms	
T_{PLL}	PLL0 Locking time		190		us	
T_{bus_rst}	Bus reset release time		10.8		us	

6. Thermal information

Table 29 - Thermal information: FCCSP 9x9

Package	Power(W)	θJA(℃ /W)	θJB(℃ /W)	θJC(℃ /W)
FCCSP 9x9		20.6 @ 0 m/s	6.07	0.9

The testing JEDEC PCB is based on 4 layers, 101.5 x 114.5 mm, 1.6 mm Thickness (**JEDEC JESD51-9)**

Table 30 - Thermal information: FCCSP 11x11

Package	Power(W)	θJA(℃ /W)	θJB(℃ /W)	θJC(℃ /W)
FCCSP		19.6 @ 0 m/s	6.12	0.88

The testing JEDEC PCB is based on 4 layers, 101.5 x 114.5 mm, 1.6 mm Thickness **(JEDEC JESD51-5)**

7. Package information

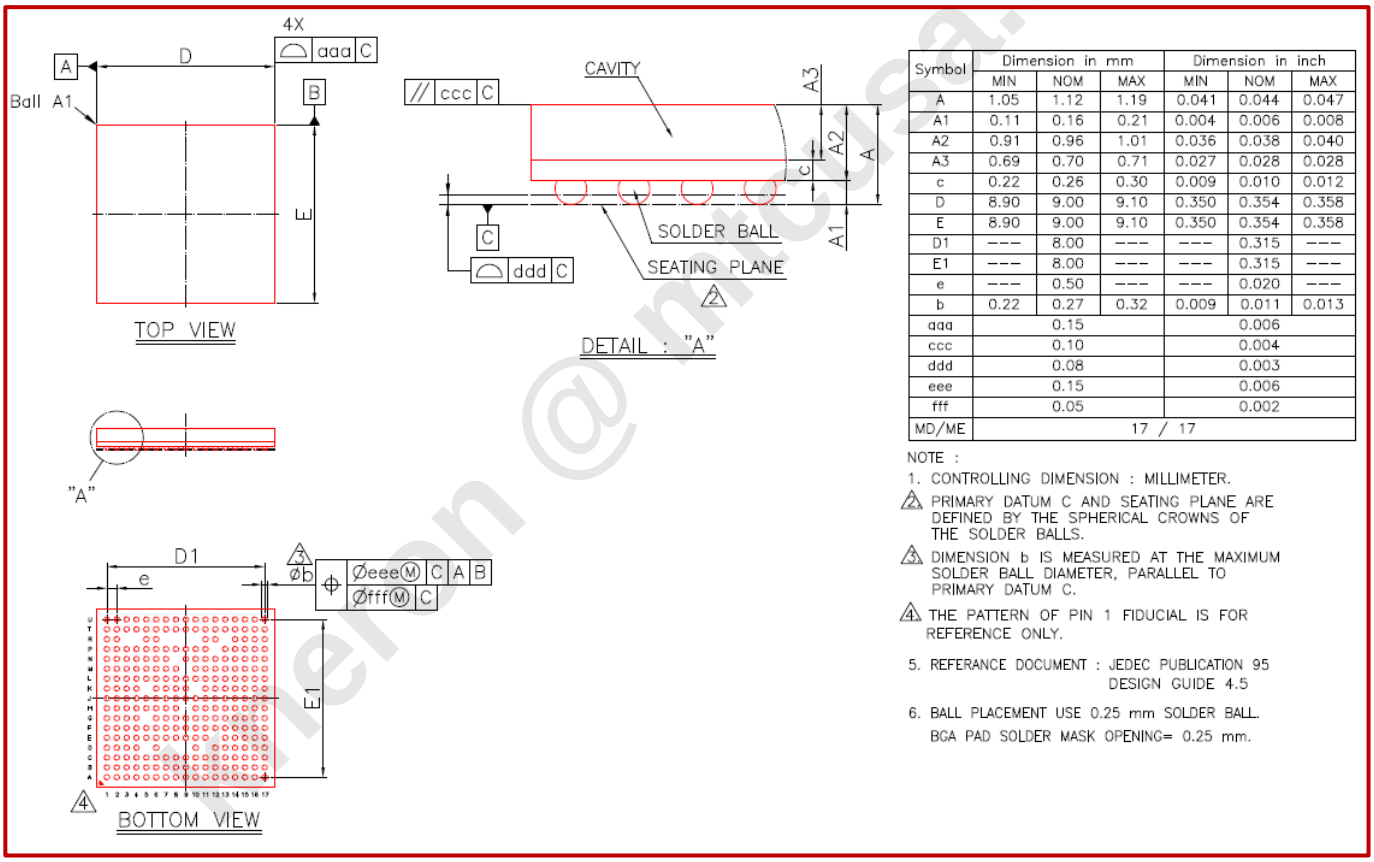
7.1 Package Information

Table 31 – Package Information

Kneron P/N	Package General Description	Environmental	MSL
KL720B3421B	FCCSP 9x9 269B, 1Gb	RoHS & REACH Compliant	Level 3
KL720B4421B	FCCSP 11x11 386B, 1Gb	RoHS & REACH Compliant	Level 3

7.2 Package Dimension

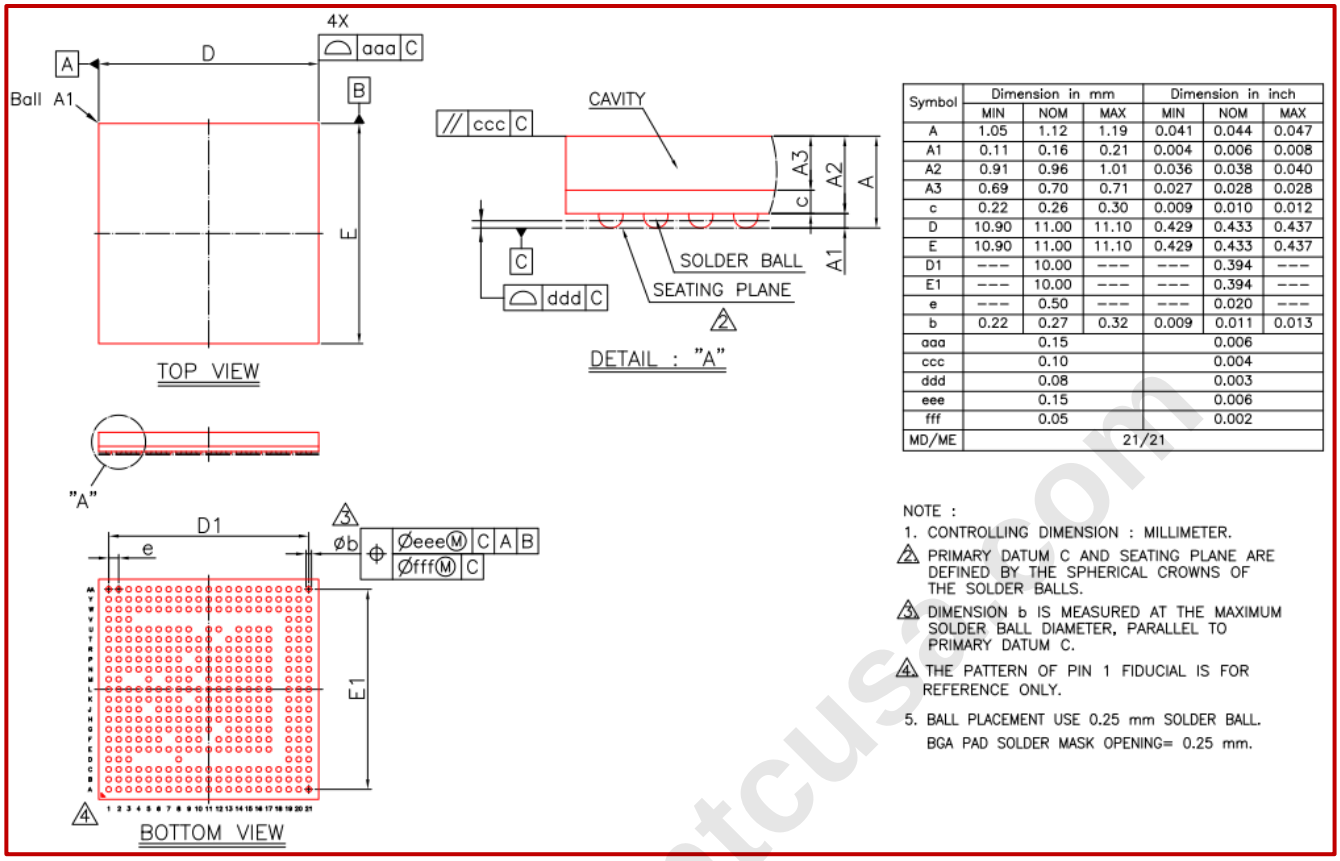
Figure 11 - FCCSP 9x9 Package



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.12	1.19	0.041	0.044	0.047
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.91	0.96	1.01	0.036	0.038	0.040
A3	0.69	0.70	0.71	0.027	0.028	0.028
c	0.22	0.26	0.30	0.009	0.010	0.012
D	8.90	9.00	9.10	0.350	0.354	0.358
E	8.90	9.00	9.10	0.350	0.354	0.358
D1	---	8.00	---	---	0.315	---
E1	---	8.00	---	---	0.315	---
e	---	0.50	---	---	0.020	---
b	0.22	0.27	0.32	0.009	0.011	0.013
aaa		0.15			0.006	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME	17 / 17					

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. REFERANCE DOCUMENT : JEDEC PUBLICATION 95 DESIGN GUIDE 4.5
6. BALL PLACEMENT USE 0.25 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING= 0.25 mm.

Figure 12 - FCCSP 11x11 Package

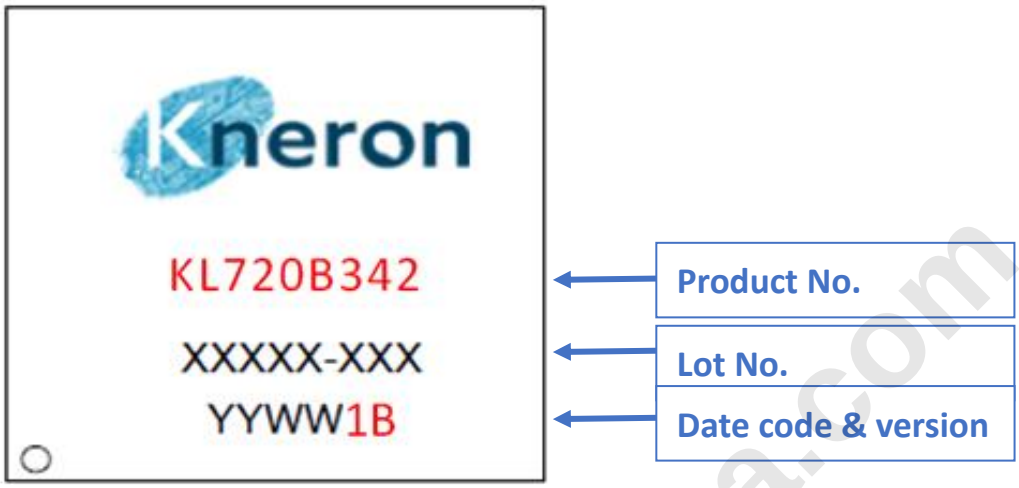


Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.05	1.12	1.19	0.041	0.044	0.047
A1	0.11	0.16	0.21	0.004	0.006	0.008
A2	0.91	0.96	1.01	0.036	0.038	0.040
A3	0.69	0.70	0.71	0.027	0.028	0.028
c	0.22	0.26	0.30	0.009	0.010	0.012
D	10.90	11.00	11.10	0.429	0.433	0.437
E	10.90	11.00	11.10	0.429	0.433	0.437
D1	---	10.00	---	---	0.394	---
E1	---	10.00	---	---	0.394	---
e	---	0.50	---	---	0.020	---
b	0.22	0.27	0.32	0.009	0.011	0.013
aaa		0.15			0.006	
ccc		0.10			0.004	
ddd		0.08			0.003	
eee		0.15			0.006	
fff		0.05			0.002	
MD/ME		21/21				

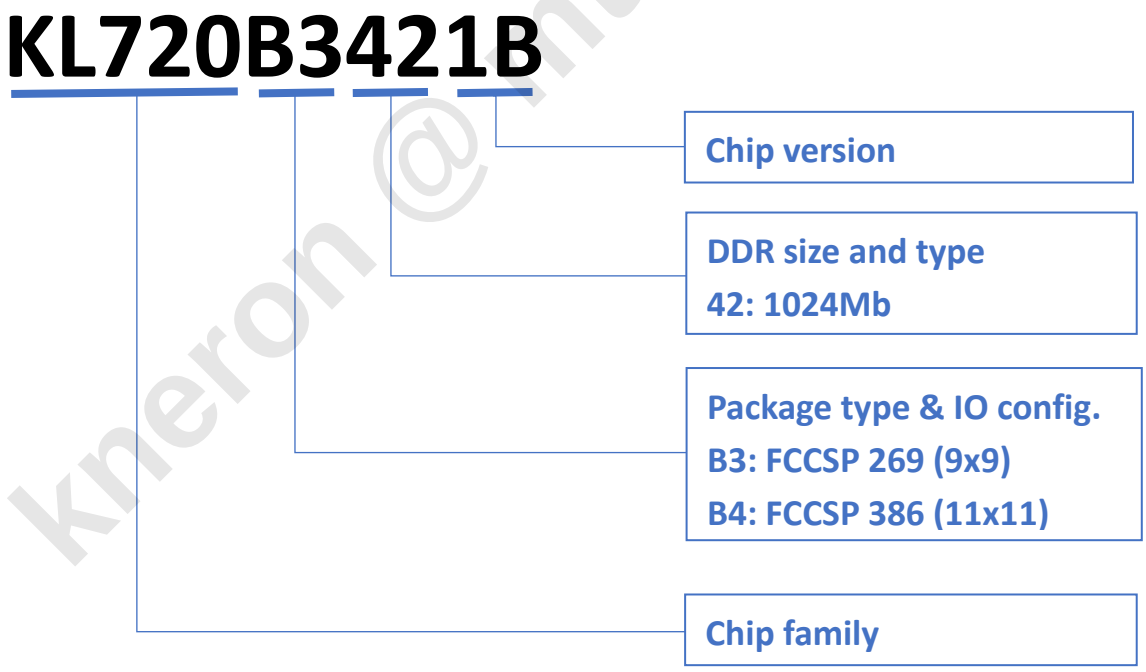
NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
5. BALL PLACEMENT USE 0.25 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING= 0.25 mm.

8. Ordering information

8.1 Top marking



8.2 Ordering information



★ Note: KL720B3421A is no longer for order.

Kneron P/N	MOQ for Engineering (ea per Tray)	MOQ for MP (ea per Inner Box)
KL720B3421B	260	2600
KL720B4421B	168	1680

9. Appendix

9.1 Reflow information

Figure 13 - Reflow profile

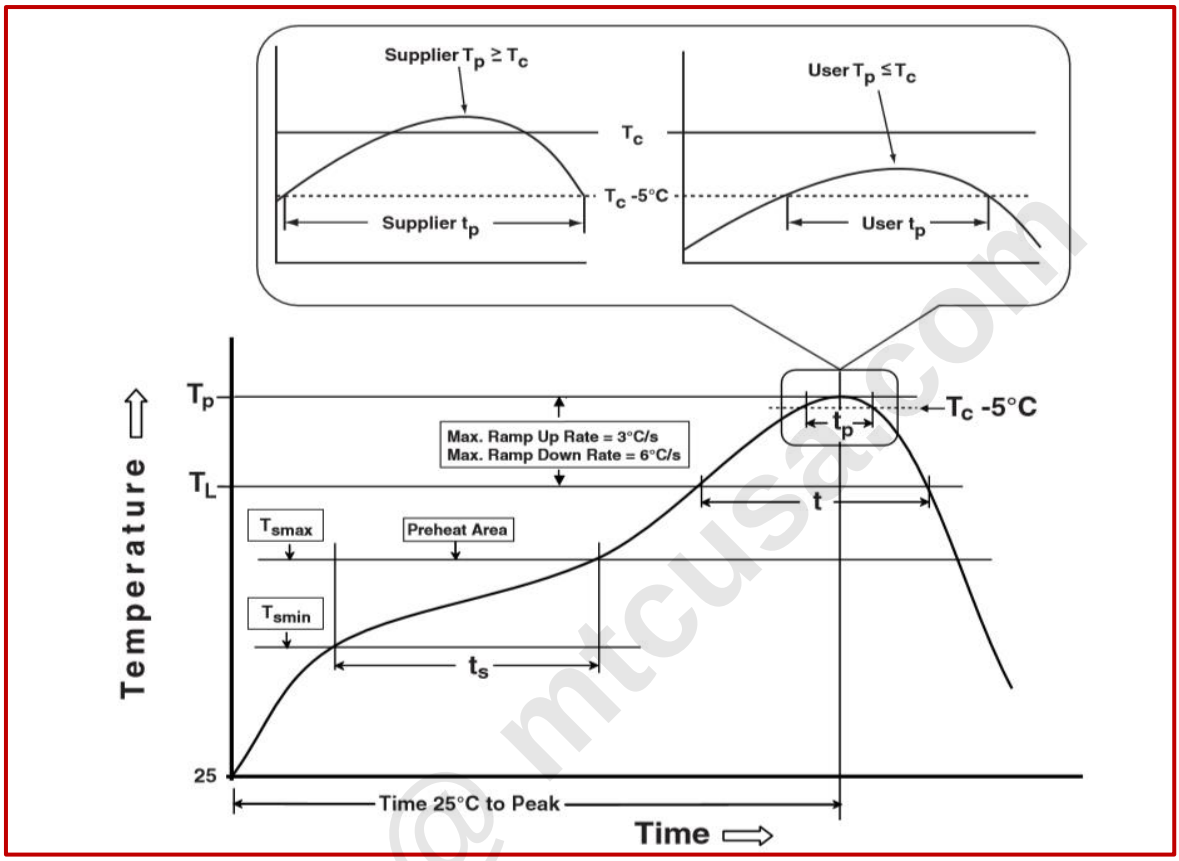


Table 32 - Classification Reflow Profiles

Profile	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat and soak		
Min. temperature (Ts_{min})	100 °C	150 °C
Max. temperature (Ts_{max})	150 °C	200 °C
Time (ts_{min} to ts_{max}) (t_s)	60 ~ 120 seconds	60 ~ 120 seconds
Average ramp-up rate (Ts_{max} to T_p)	3 °C/second (Max.)	3 °C/second (Max.)
Liquid temperature (T_L)	183 °C	217 °C
Time at liquid (t_L)	60 ~ 150 seconds	60 ~ 150 seconds
Peak package body temperature (T_p)*	Please refer to the classification temperature in Table 4.1 of IPC/JEDEC J-STD-020E – Classification Temperatures.	Please refer to the classification temperature in Table 4.2 of IPC/JEDEC J-STD-020E – Classification Temperatures.
Time (t_p)** within 5 °C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to Ts_{max})	6 °C/second (Max.)	6 °C/second (Max.)
Time to peak temperature from 25 °C	6 minutes (Max.)	8 minutes (Max.)

* Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.

** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow (e.g. live-bug). If parts are reflowed in other than the normal live-bug assembly reflow orientation (i.e. dead-bug), T_p shall be within ±2℃ of the live-bug T_p and still meet the T_c requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures, please refer to JEP140 for recommended thermocouple use.

Note 2: All components in the test load shall meet the classification profile requirements.

Note 3: SMD packages classified to a given moisture sensitivity level by using Procedures of Criteria defined within any previous version of J-STD-020, JESD 22-A112 (Rescinded), IPC-SM-786 (Rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 33 - IPC/JEDEC J-STD-020E: SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume (mm^3) <350	Volume (mm^3) ≧350
<2.5mm	235°C	220°C
≧2.5mm	220°C	220°C

Note 1: Previously classified SMDs should only be reclassified by the manufacture. Users should refer to the "Moisture Sensitivity" label on the bag to determine at which reflow temperature the SMD packages were classified.

Note 2: Unless labeled otherwise, level 1 SMD packages are considered to eb classified at 220℃.

Note 3: If supplier and user agree, components can be classified at temperatures other than those in Table of IPC/JEDEC J-STD-020E SnPb Eutectic Process and Pb-Free Process.

Table 34 - IPC/JEDEC J-STD-020E: Pb-Free Process – Classification Temperatures (Tc)

Package Thickness	Volume (mm^3) <350	Volume (mm^3) 350~2000	Volume (mm^3) ≧350
<1.6mm	260°C	260°C	260°C
1.6mm~2.5mm	260°C	250°C	245°C
≧2.5mm	250°C	245°C	245°C

Note 1: At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak body temperature (T_p) can exceed the values specified in the Table of IPC/JEDEC J-STD-020E SnPb Eutectic Process and Pb-Free Process. the use of higher T_p does not change the classification temperature T_c.

Note 2: Package volume excludes external terminates (e.g. balls. Bumps. Lands, leads) and/or nonintegral heat heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection flow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Table of IPC/JEDEC J-STD-020E - SnPb Eutectic Process and this appendix, whether or not Pb-free.

Note 5: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112 (rescinded), IPC-SM-786 (rescinded) do not need to be reclassified to the current version unless a change in classification level or a higher peak classification temperature is desired.